Project 1: Cache Controller – Interface Specifications

CPU

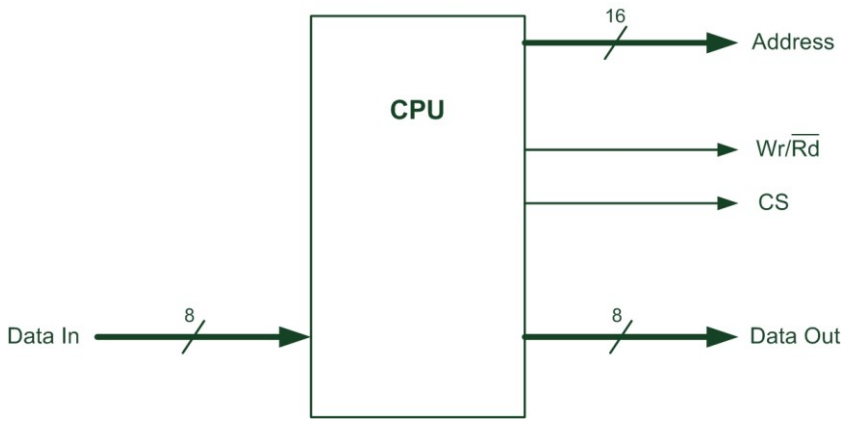

Figure 1: CPU Interface

DRAM Controller

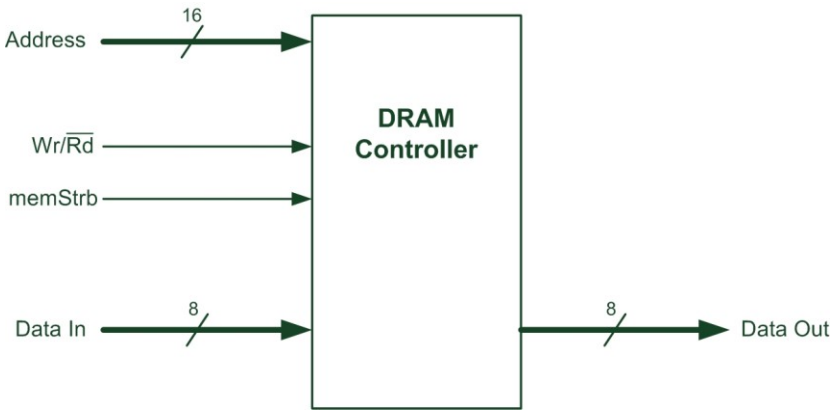

Figure 2: DRAM Controller Interface

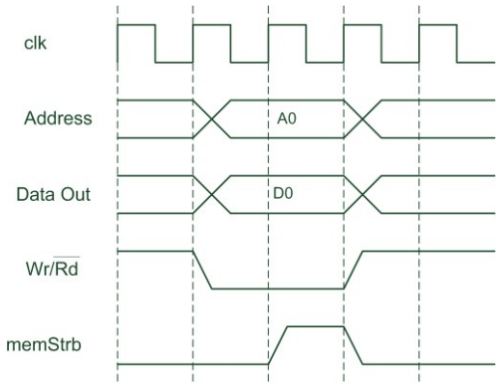

Figure 3: DRAM Single Read

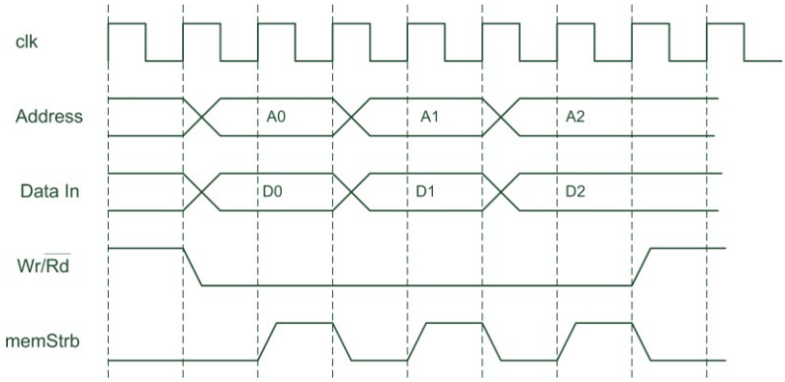

Figure 4: DRAM Block Read

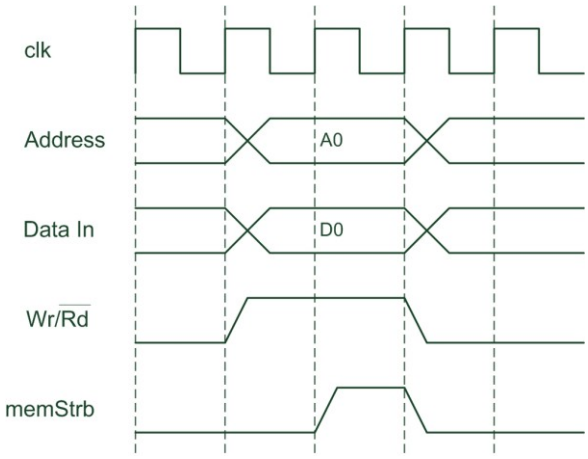

Figure 5: DRAM Single Write

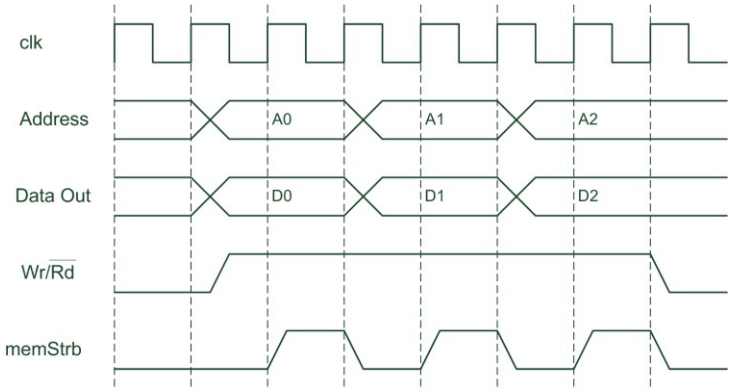

Figure 6: DRAM Block Write

CPU Component

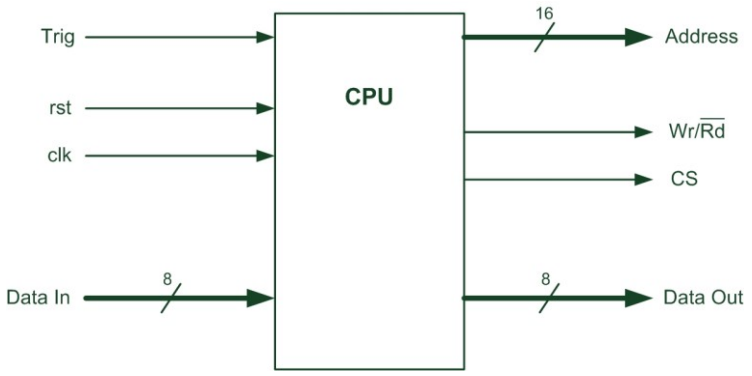

Figure 7: CPU Component Symbol

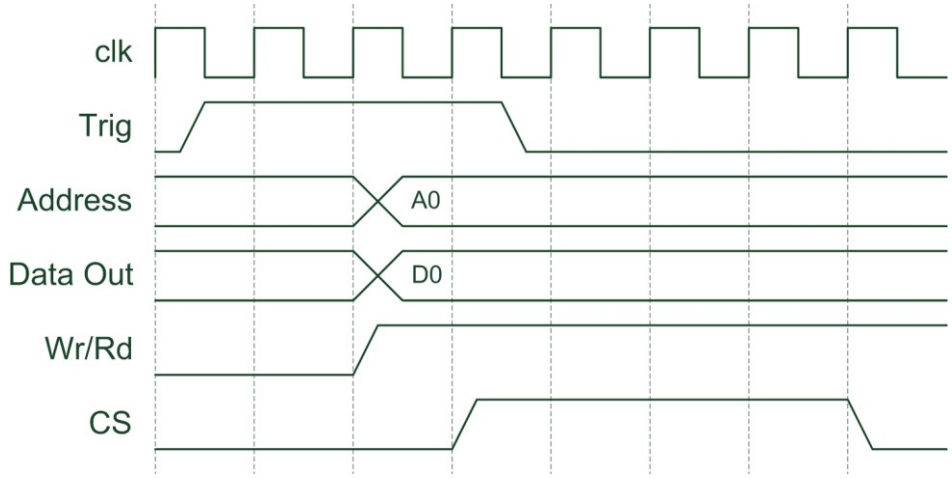

Figure 8: CPU Component Transaction