COE758 – Digital Systems Engineering

Project #1 – Laboratory Equipment

Lab Equipment Description

The laboratory platform boards found in ENG412 are designed to allow students to program and test their VHDL designs from the Altera MAX PLUS II environment. The board consists of a BIT BLASTER connected to the serial port of the UNIX workstation and provides support for programming the **Altera MAX7128SLC84** CPLD device directly from the MAX PLUS II software. In order to simulate real life conditions, a **Xilinx XC9536** CPLD is used to generate test vectors such as 8-bit data strobes, or instruction counters. To verify the proper behavior of the programmed device, students will make use of the Agilent LogicWave logic analyzer that is present under the Windows (sunPC) bootable environment.

Pinout Table

The MAX7128SLC84 is a Programmable Logic Device based on EEPROM technology and does not lose the user program during a power down or reset. In order to program the device, it is necessary to assign the appropriate pin locations using the MAX PLUS II software. The test vectors are generated by the Xilinx XC9536 CPLD for the CACHE controller project which produces a 16-bit wide counter (to be used as the CPU address). The input pinouts of the board are summarized below in Table 1. The Channel Input field represents logic analyzer input channels (**POD2**). The remaining two fields represent the appropriate signals that are to be assigned to the pins of the MAX7128SLC84 device.

Channel Input	Altera Input Signal	Floorplan Editor Device Pin #		Channel Input	Altera Input Signal	Floorplan Editor Device Pin #
0	CPU_ADDR(0)	54		9	CPU_ADDR(9)	65
1	CPU_ADDR(1)	55		10	CPU_ADDR(10)	67
2	CPU_ADDR(2)	56		11	CPU_ADDR(11)	68
3	CPU_ADDR(3)	57		12	CPU_ADDR(12)	69
4	CPU_ADDR(4)	58		13	CPU_ADDR(13)	70
5	CPU_ADDR(5)	60		14	CPU_ADDR(14)	73
6	CPU_ADDR(6)	61		15	CPU_ADDR(15)	74
7	CPU_ADDR(7)	63			CLOCK	83
8	CPU_ADDR(8)	64				

Table 1: Input pin assignments

The output pinouts of the board are summarized below in Table 2. The Channel Output field represents logic analyzer output channels (**POD1**). The remaining two fields represent the appropriate signals that are to be assigned to the pins of the MAX7128SLC84 device.

Channel Output	Altera Output Signal	Floorplan Editor Device Pin #		Channel Output	Altera Output Signal	Floorplan Editor Device Pin #
0	SRAM_ADDR(0)	11		8	OE	22
1	SRAM_ADDR(1)	12		9	TAG_0	24
2	SRAM_ADDR(2)	15		10	TAG_1	25
3	SRAM_ADDR(3)	16		11	TAG_2	27
4	SRAM_ADDR(4)	17		12	TAG_3	28
5	SRAM_ADDR(5)	18		13	TAG_4	29
6	SRAM_ADDR(6)	20		14	TAG_5	30
7	WE	21		15	TAG_6	31

Table 2: Output pin assignments

Notes

- You should attempt to write your VHDL code as efficiently as possible. (i.e., avoid many nested IF statements and large numerical comparisons)
- Please set "**Multi-level Synthesis for MAX7000 Devices**" in the **Global Logic Synthesis** option under **#ASSIGN#**
- You must ensure that your design *does not use more than **128 logic cells*** otherwise your project will not fit within the design!! To see how many logic cells your design uses, read the report generated by the **#FITTER#** during the compilation stage.