RYERSON UNIVERSITY
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING
ELE734: LOW-POWER DIGITAL INTEGRATED CIRCUITS

COURSE OUTLINE
September 2012

Course Description: This course deals with the design of Digital CMOS integrated circuits. The course consists of three essential components: Theory, Laboratory, and project. Variety of design techniques, such as Static CMOS, Dynamic CMOS, and Transmission Gate are discussed in theory. These designs are studied on basic logic gates as well as combinational and sequential circuits. The lessons learned are applied to arithmetic building blocks such as adders, multipliers, and memory elements. A MOS transistor is studied using I-V equations, and the different areas of operations are modeled. The static (DC) are dynamic (transient) behaviors for an important building block, a CMOS inverter, are studied in depth.

Prerequisite: ELE 504, ELE 531, ELE 532, MTH 514, ELE 635, ELE 639, MEC 511 and (ELE 538 or COE 538)

Course hours: Lecture: 3 hours/week; Lab 2 hours/week

Course Evaluation:	**Theory**	**65%**	**Laboratory**	**35%**
	Mid-term test	25	Lab 1	10
	Final Exam	40	Lab 2	7
			Lab 3	10
			Lab 4	8

- The mid-term test and final examination will be closed book.
- **In order to achieve a passing grade in this course, the student must achieve an average of at least 50% in both theoretical and laboratory components.**
- The written reports will be assessed not only on their technical or academic merit, but also on the communication skills of the author as exhibited through the reports.

Text: CMOS VLSI Design: A Circuit and Systems Perspective, Neil H. E. Weste and David Harris (ISBN: 0-321-14901-7)

Lab manual: ELE734 Low Power Digital Integrated Circuits Laboratory Manual, Adnan Kabbani and Tarek Khan (posted on blackboard).

Website: Blackboard http://www.my.ryerson.ca

Course Instructor: Dr. Andy Ye, Office ENG319, Tel: 416 979 5000 ext. 4901, email: aye@ee.ryerson.ca .

Lecture and Lab schedules, Fall 2012

Week	Lecture Topic	Experiment/Tutorial
Week-1 **Sep 4 – Sep 10, 2012**	**Introduction to the Course** **Lab Description**	**No Lab or Tutorial** **(Lab Starts in the Week of Sep 10 – Sep 16)**
Week-2 **Sep 11 – Sep 17, 2012**	**Introduction** **Chap-1, sections: 1.1 to 1.11**	**Lab 1: Characteristics of MOSFET Devices**
Week-3 **Sep 18 – Sep 24, 2012**	**MOS Transistor Theory** **Chap-2, sections: 2.1 to 2.5**	**Lab 1: Characteristics of MOSFET Devices (Continued)**
Week-4 **Sep 25 – Oct 1, 2012**	**CMOS Processing Technology** **Chap-3, sections: 3.1 to 3.6**	**Lab 1: Characteristics of MOSFET Devices (Continued)**
Week-5 **Oct 2 – Oct 15, 2012 (Including Fall Study Week)**	**Delay** **Chap-4, sections: 4.1 to 4.6**	**Lab 2: CMOS Inverter Design**
Week-6 **Oct 16 – Oct 22, 2012**	**Power** **Chap-5, sections 5.1 to 5.6**	**Lab 2: CMOS Inverter Design (Continued)**
Week-7 **Oct 23 – Oct 29, 2012**	**Mid-Term Test: Tuesday, Oct 23**	**No Lab – Midterm**
Week-8 **Oct 30 – Nov 5, 2012**	**Interconnect** **Chap-6, section 6.1 to 6.5**	**Lab 3: CMOS Logic Families**
Week-9 **Nov 6 – Nov 12, 2012**	**Robustness** **Chap-7, sections: 7.1 to 7.6**	**Lab 3: CMOS Logic Families (Continued)**
Week-10 **Nov 13 – Nov 19, 2012**	**Circuit Simulation** **Chap-8, sections: 8.1 to 8.6**	**Lab 3: CMOS Logic Families (Continued)**
Week-11 **Nov 20 – Nov 26, 2012**	**Combinational Circuit Design** **Chap-9, sections: 9.1 to 9.6**	**Lab 4: 1-bit CMOS Full Adder**
Week-12 **Nov 27 – Dec 3, 2012**	**Sequential Circuit Design** **Chap-10, sections: 10.1 to 10.7**	**Lab 4: 1-bit CMOS Full Adder (Continued)**