Stratix
FPGA Family

November 2002, ver. 2.2 Errata Sheet

This errata sheet provides updated information on Stratix™ engineering sample (ES) devices. Altera has identified four silicon issues affecting these devices. This document addresses the issues and includes methods to work around the issues.

Table 1 shows these issues and which Stratix devices each issue affects.

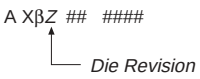
Table 1. Stratix Family Issues

Issue	Affected Devices	Fixed Devices
Configuration control block silicon issue	EP1S10 ES devices	EP1S10 production devices
I/O element (IOE) register synchronous clear and preset	EP1S25 revision A and B devices	EP1S25 revision C and later devices
Release clears before tri-state	EP1S25 revision A and B devices	EP1S25 revision C and later devices
High current on power up	EP1S10 ES devices EP1S25 ES devices	*(1)* EP1S25 production devices
Terminator technology (R_{UP}/R_{DN} pin) issue	EP1S40 ES devices	EP1S40 production devices
Gated lock (GLOCK)	All Stratix devices	*(2)*
Phase-locked loop (PLL) switchover	All Stratix devices	*(3)*

Notes to Table 1:
(1) Contact Altera Applications for information on EP1S10 devices regarding this problem.
(2) Altera is offering a work around for this feature. See "Gated Lock (GLOCK)" on page 4 for more information.
(3) Altera is offering a work around for this feature. See "PLL Switchover Glitch" on page 6 for more information.

The die revision is identified by the alphanumeric character (Z) before the fab code (first two alphanumeric characters) in the lot number printed on the top side of the device. Figure 1 shows a Stratix device's top side lot number.

Figure 1. Stratix Device Top Side Lot Number



EP1S10 Device Issue

There is a silicon issue in the control block circuitry that affects all modes of configuration, requiring a software change in the Quartus® II configuration algorithms for ES devices.

The Quartus II software version 2.1 SP1 will enable correct configuration support for EP1S10 ES devices. The Quartus II software version 2.1 SP1 will have both an ES and production ordering code for EP1S10 devices. When targeting EP1S10 ES devices, the Quartus II software version 2.1 SP1 will generate correct configuration files for the ES devices. Designers should use the ES ordering code in the Quartus II software for configuring ES devices and the production ordering codes for configuring production devices. When targeting the production ordering code, the Quartus II software version 2.1 SP1 does not generate configuration files. The Quartus II software will provide full support when production devices are available.

The EP1S10 device Serial Object File (**.sof**) size will remain the same as the production file. The configuration algorithm that accesses the **.sof** file and configures the device(s) contains updated information that allows the EP1S10 devices to configure correctly. All other configuration files contain overhead bits that identify the device as an EP1S10 device. Programmer Object File (**.pof**), Raw Binary File (**.rbf**), Tabular Text File (**.ttf**), and Hexidecimal File (**.hex**) programming files for revision A and B devices have a larger file size because of the required changes in the overhead bits. The files generated by the Quartus II software version 2.1 SP1 for EP1S10 ES devices will be larger than documented production file sizes.

EP1S25 Device Issues

The following silicon issues only affect the EP1S25 ES devices:

- IOE register synchronous clear and preset
- `RELEASE_CLEARS_BEFORE_TRI_STATES` logic option

IOE Register Synchronous Clear and Preset

Synchronous clear and preset signals cannot be used on IOE input registers.

Contact a local Altera FAE or Altera Applications for software support on this issue.

Release Clears Before Tri-States

When the RELEASE_CLEARS_BEFORE_TRI_STATES option is used, registers clocked by internal global clock nets (including PLL outputs) will power up in an unknown state instead of the state specified by the user.

When the RELEASE_CLEARS_BEFORE_TRI_STATES option is turned on, the designer must reset the device to operate correctly.

The RELEASE_CLEARS_BEFORE_TRI_STATES configuration option directs the device to release the clear signal on registered logic cells and I/O cells before releasing the output enable override on tri-state buffers. If this option is turned off, the output enable signals are released before the clear overrides are released. This option will be turned off by default. When the designer turns this option on, the Quartus® II software generates the following warning message: "Release clears before tri-states option is turned on. If you are using ES silicon, contact Altera Applications."

EP1S10 & EP1S25 High Power-Up Current Issue

EP1S10 ES devices typically require a 750-mA current on the V_{CCINT} voltage supply to successfully power up. EP1S25 ES devices typically require a 2.5-A current on the V_{CCINT} voltage supply to successfully power up the device. Designers should select power supplies and regulators that can supply this amount of current when designing with EP1S10 and EP1S25 ES devices.

The production EP1S25 devices are fixed and require significantly less power-up current.

EP1S40 Device Issue

Altera has identified a routing issue with the 8 pins on EP1S40 ES devices listed in Table 2. These 8 pins include R_{UP} and R_{DN} pins. As a result, Stratix EP1S40 ES devices do not support on-chip termination via the terminator technology feature on the top and bottom banks (banks 3, 4, 7, and 8). Designers can still use these pins as I/O pins.

Table 2 shows pins from the EP1S40 device pin outs affected by this issue.

Table 2. EP1S40 ES Device Affected Pins

Pin Name/Function	Optional Function	Pin Number		
		956-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
IO	RDN8	AE23	AC20	AH24
IO	RUP8	AG25	AH19	AF23
IO	RDN7	AG14	AC14	AP17
IO	RUP7	AF13	AF13	AN16
IO	RUP4	F13	G13	F15
IO	RDN4	E14	J13	E16
IO	RUP3	F22	F21	P23
IO	RDN3	F24	L19	M24

Production EP1S40 devices have correct pin connections and comply with the EP1S40 pin table. When designing with Stratix EP1S40 ES devices, designers must use the EP1S40 ES ordering codes in the Quartus II software version 2.2. When using with production devices, the design must target the production EP1S40 ordering codes.

Designers must recompile their designs when moving from ES to production devices. The Quartus II software version 2.2 will provide advanced support for EP1S40 production devices. Designers will need to contact their local Altera representative to obtain software support for configuration file generation.

Stratix Family Issues

The following issues affect all Stratix devices.

- Gated lock (GLOCK)
- PLL switchover glitch

Gated Lock (GLOCK)

The enhanced PLL includes a programmable counter that holds the lock signal low for a user-selected number of input clock transitions. This allows the PLL to lock before enabling the lock signal.

There is a run-through problem in the GLOCK counter that causes the counter to operate incorrectly. Support for the gated lock circuitry was disabled in the Quartus II software version 2.1. Therefore, the gated lock feature is unavailable in Stratix devices.

The work around for this problem is to gate the lock signal in internal logic. Altera recommends using a two-input AND gate to gate the lock signal with a counter. The counter determines how many clock cycles before the lock signal is released. See Figure 2.

Figure 2. Gated Lock in Internal Logic Circuit

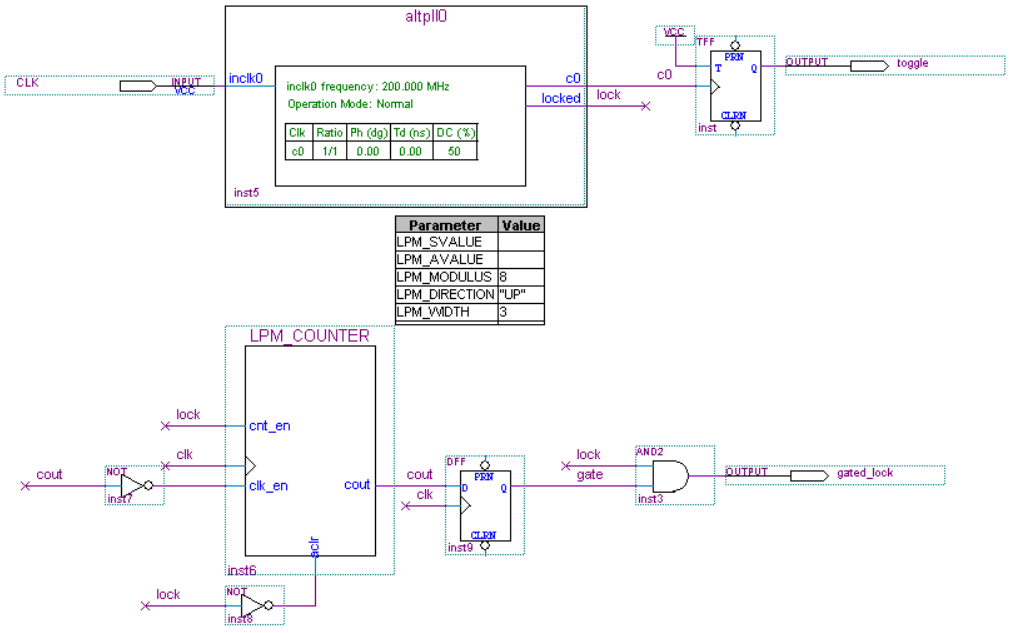
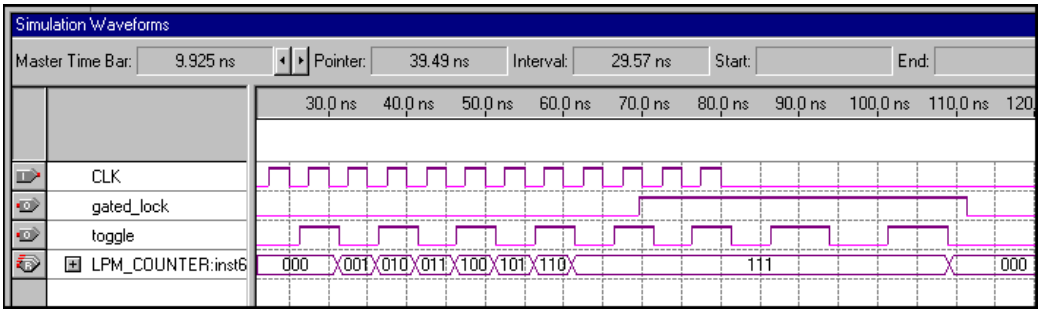


Figure 3 shows the simulation waveform of the gated lock signal.

Figure 3. Gated Lock Signal Simulation Waveform



PLL Switchover Glitch

The CLKBAD0 and CLKBAD1 signals have a design flaw that causes a glitch in the signals. The glitches last for a half clock cycle. CLKBAD0 and CLKBAD1 are available for designers to use to control switchover internally.

To work around this issue, the designer should implement the circuit shown in Figure 4 to monitor the CLKBAD signal of the primary clock and initiate a switchover when the primary clock fails. The CLKBAD signal must be high for four clock cycles (the two-bit counter reaches four) before the circuit switches to the secondary clock. The counter will be cleared if there is a glitch in the CLKBAD signal it goes low in error before the counter reaches four. The CLKBAD signal is registered before driving the counter's cnt_en signal to prevent metastability. The clkswitch signal is latched so that it will only trigger a switch from the primary clock to the secondary clock.

In the circuit shown in Figure 4, CLK0 is the primary clock and CLK1 is the secondary clock. The circuit monitors the CLKBAD0 signal to determine when the clock driving CLK0 is lost.

Figure 4. Clock Switchover Circuit

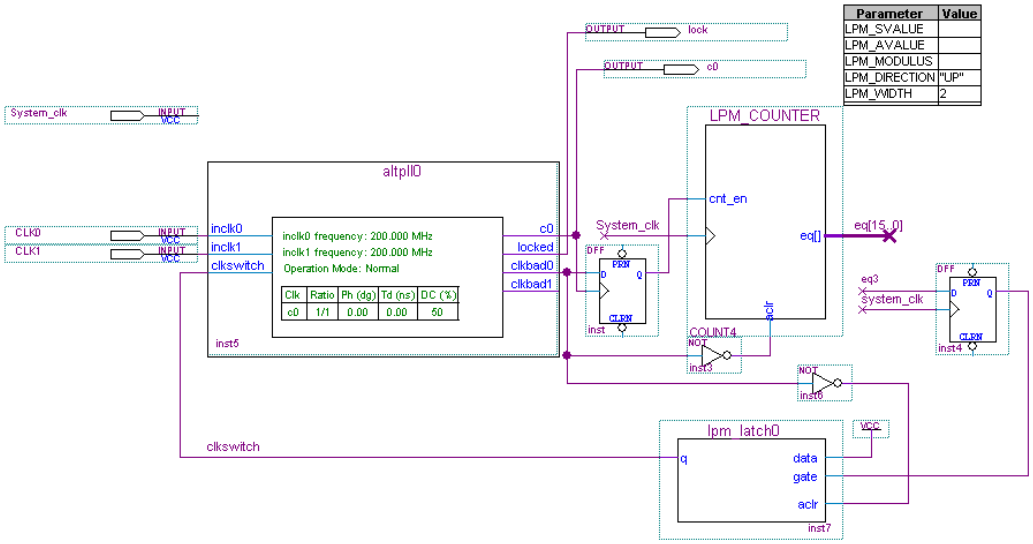
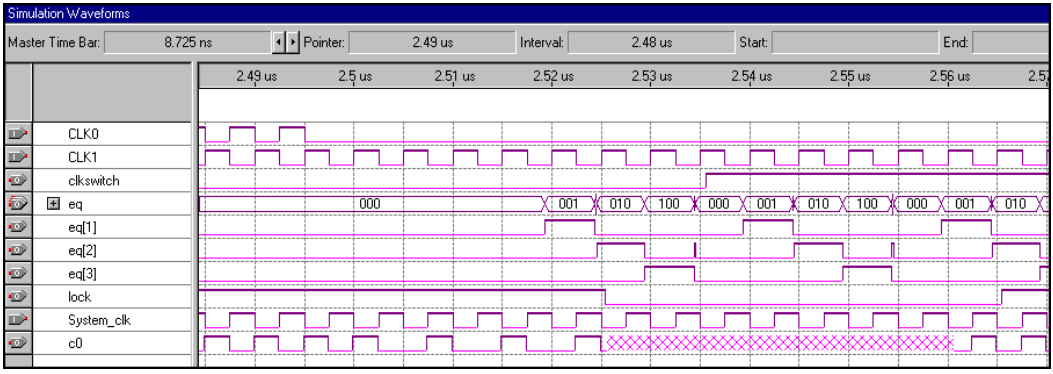


Figure 5 shows the simulation waveform of the PLL switching over from CLK0 to CLK1 when the input CLK0 is lost.

Figure 5. Simulation Results of Switchover Event



Revision History

The information contained in the *Stratix Programmable Logic Device Family Errata Sheet* version 2.2 supersedes information published in previous versions.

Version 2.2

The *Stratix Programmable Logic Device Family Errata Sheet* version 2.2 contains the following changes:

- Updated Table 1.
- Added "EP1S40 Device Issue" on page 3.

Version 2.1

The *Stratix Programmable Logic Device Family Errata Sheet* version 2.1 contains the following changes:

- Updated Table 1.
- Added "EP1S10 & EP1S25 High Power-Up Current Issue" on page 3.
- Updated Figures 4 and 5.

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