COE838: Systems-on-Chip Design
Sample Midterm Exam

Name and Student ID: _____

Total Time Allowed: 9**0 Minutes** Maximum Marks:5**0**

i. The examination has 5 pages and 5 questions. Answer all the questions. State any **assumptions**.
ii. To earn maximum credit, your answer must be concise, to the point and in the given space
iii. All questions are not of the same difficulty and value. Consider this when allocating time for their solutions.

1. An SoC application has 6 tasks (T1, T2, T3, T4, T5 and T6) shown in Fig 1(a)'s DFG. Fig 1(b) displays the SoC architecture employed in the system's design. The SoC consists of a processor (CPU), an accelerator (ACC), and a dual-port memory. The memory is used for sharing data between the accelerator and CPU, with the accelerator and CPU containing their own internal memories.

   Consider offloading and communication costs in the architecture, where every bus transaction between the CPU and accelerator endure a 10 clock cycle latency (including writing and reading to the memory for every transaction). Specific execution times for each core are given in Table I. Assume no startup costs.

   Determine and clearly state the optimal task mapping for the DFG, and the scheduling diagram so that the SoC completes its tasks in the least time possible. Show all your work.

Table I: Task Execution Times

Task	CPU (us)	ACC (us)
T1	50	25
T2	40	20
T3	20	10
T4	10	-
T5	-	5
T6	30	15

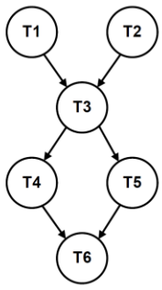

Fig. 1(a): Application DFG

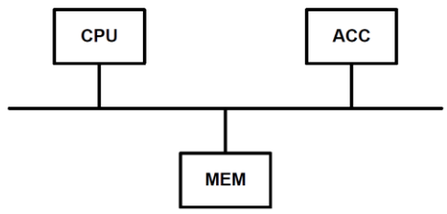

Fig. 1(b): SoC Architecture

MARKS: 10

(Extra Space Provided)

2. Convert the following VHDL based system of a revised 32-bit T flip flop into its SystemC equivalent. Write your solution in the code templates provided below.

```
library ieee;
use ieee.std_logic_1164.ALL;
ENTITY tff IS
     port(clk, rst       : IN STD_LOGIC;
          t              : IN STD_LOGIC;
          en             : IN STD_LOGIC;
          q, q_bar       : BUFFER STD_LOGIC_VECTOR(31 DOWNTO 0));
END tff;

ARCHITECTURE description OF tff IS
BEGIN
       IF(rst = '1')THEN
              q <= (OTHERS => '0');
              q_bar <= (OTHERS => '1');

       ELSE IF(rising_edge(clk)) THEN
              IF(en = '1')THEN
                     if(t = '1') then
                            q <= q_bar;
                            q_bar <= q;
                     end if;
              END IF;
       END IF;
END description;
```

MARKS: 10

tff.h

```
#include <systemc.h>

SC_MODULE(tff){
```

tff.cpp

```
#include "tff.h"

void tff :: tff_method(){
```

3. You are required to develop a Set-Top Box SoC which inputs a signal and transforms the data to content displayed on a TV screen. Consider a wafer yield of 98%, and a defect density of 0.1 per square cm. The target feature size is at the 65nm technology node. The Set-Top Box SoC architecture must consist of the following components:

Unit	Area (A)
64b CISC processor with 48KB of I-cache and 32KB of D-cache	300
A Texas Instrument DSP (for video signal acquisition)	150
A SHARC-based DSP (for demodulation/ error correction schemes)	185
MPEG-2 transport stream de-multiplexer accelerator unit	215
Bus and bus control	400
Application Memory (512KB)	1024
Shared SRAM L2 cache	

Assume 11% chip area for net die costs i.e. IO pads etc, and 12% overhead integration for connecting the shared L2 cache to the rest of the components in the SoC. **Generate an architecture and floorplan for this SoC.** Show all calculations and the steps undergone to implement your design. Specify all component areas, and the final capacity (actual and practical) of the SRAM L2 cache your system may support.

MARKS: 15

4. Briefly describe the importance of the dont_initialize() function in a SystemC constructor. Give an example of why and how it may be used.

MARKS: 4

5. a) What is pipelining?
   b) Why would pipelining be required in a digital system?
   c) What limits the frequency of a pipeline? How could the frequency be increased?

MARKS: [2 + 2 + 3]

d) What is a bitstream? How does it differ from a standard compiled software program?

MARKS: 4