# Problem-Set #4
## COE 608: Computer Organization and Architecture
## Multicycle MIPS-Lite CPU and Pipelining

## (a) MIPS-Lite CPU Multi-Cycle Control and Pipelining

Chapter 4:

Exercises: 4.12, 4.13, 4.14, 4.16, 4.17, 4.18, 4.19, 4.20, 4.21 and 4.22.1 & 4.22.2.

Additional Questions

**Q.1.** How could we modify the following code to make use of a delayed branch slot?

```
Loop:   lw $2, 100($3)
        addi $3, $3, 4
        beq $3, $4, Loop
```

**Q.2.** Identify all the data dependencies in the following code.
Which dependencies are data hazards that can be resolved by forwarding?

```
add $2, $5, $4
add $4, $2, $5
sw  $5, 100($2)
add $3, $2, $4
```