Problem-Set #2
COE 608: Computer Organization and Architecture
Computer Performance and Register Transfer

a. Computer Performance

Chapter 1: Exercises: 1.3, 1.4, and 1.5.

Additional Exercises:

1. Consider an application program AP, which runs on a 1 GHz system S in 10 seconds. An optimization is made to AP, replacing all instances of multiplying a value by 4 (e.g. MULT Y, Y, 4) with two instructions of addition (ADD Y, Y). The new optimized application program is called NAP. The CPI of MULT instruction is 4, and the CPI of an ADD is 1. After re-compiling , the new program, NAP runs in 9 seconds on the system S. How many multiplies were replaced by the new compiler?
2. Assume that divide instructions take 12 cycles and account for 15% of the instructions in a program, while the other 85% of instructions require an average of 4 cycles for each instruction. What percentage of time does the CPU spend doing division?
3. The hardware engineering team has claimed that they can reduce the number of cycles for division to 8 in Exercise 2. However, this change will require a 20% increase in the clock cycle time and nothing else will be affected by this change. Should they proceed with the modification?

b. Register Transfer

4. Implement the logic to facilitate the following Register Transfers among the registers R0, R1 and R2. The control variables are mutually exclusive i.e. only one variable can be HIGH at any time, while the other two are LOW.

   Ca: R1 ← R2 ; R0 ← R2
   Cb: R2 ← R0
   Cc: R0 ← R1 ; R2 ← R1

   (a) Using Registers and dedicated multiplexers, draw a detailed logic diagram of the hardware implementing a single bit of these register transfers.
   (b) Draw a logic diagram of a simple logic circuit whose inputs are the control variables. The circuit generates the select signals for the multiplexers and load signals for registers.

5. Design a 4-bit arithmetic circuit with two select variables S1 and S0 that generates the following arithmetic operations in conjunction with a control signal Cin.

S_1 S_0	Cin = 0	Cin = 1
0 0	F = A + B (add)	F = A + B + 1
0 1	F = A (transfer)	F = A + 1 (increment)
1 0	F = B' (complement)	F = B' + 1 (negate)
1 1	F = A + B'	F = A + B' + 1 (subtract)

Draw the logic diagram for a single-bit stage