Problem-Set #1
COE608: Computer Organization and Architecture
Introduction, Instruction Set Architecture and Computer Arithmetic
Chapters 1, 2 and **3**

a. Chapter 1: Exercises: 1.1.1 => 1.1.26

b. Chapter 2:

Exercises: 2.6, 2.12, 2.18, 2.24, 2.27, 2.30.

Questions from 3rd Edition

2.2: What binary number does this hexadecimal number represents 7FFF $FFFF_{16}$?
What decimal number does it represent ?

2.3: What hexadecimal number does this binary number represents
$1100101011111110111101011001110_{two}$?

2.4: Why doesn't MIPS have a subtract immediate instruction ?

2.32: Show the single MIPS instruction or a minimal sequence of instruction for this C statement.

```
b = 25 | a ;
```

Additional Questions:

1. Add comments to the following MIPS code and describe in one sentence what it computes. Assume that $a0 is used for the input and initially contains N, a positive integer. Assume that $v0 is used for the output:

```
begin:  addi    $t0, $zero, 0
        addi    $t1, $zero, 1
loop:   slt     $t2, $a0, $t1
        bne     $t2, $zero, finish
        add     $t0, $t0, $t1
        addi    $t1, $t1, 2
        j       loop
finish: add     $vo, $t0, $zero
```

2. Show a minimal sequence of MIPS instructions for the following C language statement.

X[10] = X[11] + c ;

Assume that **c** corresponds to register $t0 and the array **X** has a base address of $(4{,}000{,}000)_{10}$

3. For the following C language code, write an equivalent MIPS assembly language program.

```
a = b + c ;
b = a + c ;
d = a  - b ;
```

Calculate the instruction bytes fetched and the memory data bytes transferred (read and written).

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c. Chapter 3: Exercises:

3.5.1, 3.6.1, 3.6.2

Questions from 3rd Edition

3.7. Find the shortest sequence of MIPS instructions to determine the absolute value of a 2'complement integer. Convert this instruction (accepted by the MIPS assembler):

```
abs    $t2, $t3
```

3.10. Find the shortest sequence of MIPS instructions to determine if there is a carry out from the addition of two registers (register $t3 and $t4). Place a 0 or 1 in register $t2 if the carry out is 0 or 1, respectively.

3.12. Suppose that all of the conditional branch instructions except beq and bne were removed from the MIPS instruction set along with slt and all of its variants (slti, sltu, sltui). Show how to perform.

```
slt  $t0, $s0, $s1
```

using the modified instruction set in which slt is not available .

3.30. Given the bit pattern:

1010 1101 0001 0000 0000 0000 0000 0010

what does it represent , assuming that it is

a). a 2's complement integer?
b). an unsigned integer?
c). a single precision floating point number ?
d). a MIPS CPU instruction?

3.36. Add 3.63×10^4 and 6.87×10^3, assuming that you have only three significant digits.

3.37. Show the IEEE 754 binary representation for the floating point number 20_{ten} in single and double precision.

3.38. The same question as 3.37 but replace the number 20_{ten} with 20.5_{ten}.

3.39. The same question as 3.37 but replace the number 20_{ten} with the decimal fraction –5/6.

3.45. The internal representation of floating point numbers in IA-32 is 80 bits wide. This contains a 16-bit exponent. However, it also advertises a 64-bit significand. How is this possible?

Additional Questions:

1. Determine whether arithmetic overflow occurs in each of the following 8-bit 2's complement arithmetic operations.

(a)	10010010 + 00111110	(b)	00011000 - 10100000
(c)	01111111 + 00000010	(d)	10100001 - 00100101

2. Subtract $(13)_{10}$ from $(39)_{10}$ using 2's-complement arithmetic.