Ch4 questions and answers

4.1.a-values of control signals for add Rd, Rs, Rt

Regdst, jump,branch,memread, memtoreg,ALUop, memwrite, ALUsrc,Regwrite

1	0	0	0	0	100	0	0	1

b-lw Rt, offs(Rs)

Regdst, jump,branch,memread, memtoreg,ALUop, memwrite, ALUsrc,Regwrite

0	0	0	1	1	000	0	1	1

4.1.2.a-block used for add: IM, RF, ALU,

b- lw: IM, RF, ALU, DM

4.1.3.a-add : sign ext produced output not used, branch adder produced output not used

b-lw: RF RT produced output not used, branch adder produced output not used

4.1.4.a-critical path for AND: IM + RF + MUXALUsrc + ALU + MemtoReg MUX + RF write

=400+ 200+ 30+ 120 + 30 + 200=980

4.1.5.a- LD : IM + RF + MUXALUsrc + ALU + DM + MemtoReg MUX + RF write

=400+ 200+ 30+ 120 + 350+ 30 + 200= 1330

4.1.6.a- BEQ: IM + RF + MUXALUsrc + ALU + branchMUX

=400+ 200+ 30+ 120 + 30=780

4.6.1-cycle time for only fetch= IM =400

4.6.2-Cycle time for unconditional PC relative branch= IM + Adder + sign extnd + shiftleft2

=400 + 100 + 20 + 2=522

4.6.3-Cycle time for cond branch= IM + RF + AlusrcMUX + ALU + branch-mux

=400 + 200 + 30 + 120 + 30=780

4.6.4a- PC+4 is used for all instructions except jump

b-data memory is used only for lw and sw

4.7.1.a-cycle time for Rtype= IM + RF + ALUsrcMUX + ALU + MemtoReg-MUX + RF

=400+ 200 + 30 + 120 + 30 + 200= 980

4.7.2.a cycle time for lw= IM + RF + ALUsrcMUX + ALU + D.Mem + MemtoReg-MUX + RF

=400+ 200 + 30 + 120 +350+ 30 + 200= 1330

4.9.1-a-lw $1, 40($6) = 35,6,1,40=100011,00110,00001,00----101000

4.9.2.a-reg1=$6, yes it is read, register2 is read but not used

4.9.3.a-register write is $1, yes it is written to

4.9.4-a-Regdst=0 for lw

4.11.1.a-instruction is lw $3, 16($2)

Sign ext output=00000000---10000 32 bit

4.11.2.a-ALU inputs = $2 , 16 extended

4.11.3.a-Next PC=PC+4

4.11.4.a-lw instruction ALU-srcMUX out=16 extended , MemtoReg MUX= mem content=0, Regdest=$3

4.11.5.a-ALU src1=$2, source2=16

4.11.6.a-RS=2, RT=3, RD=RT=3, Di=0