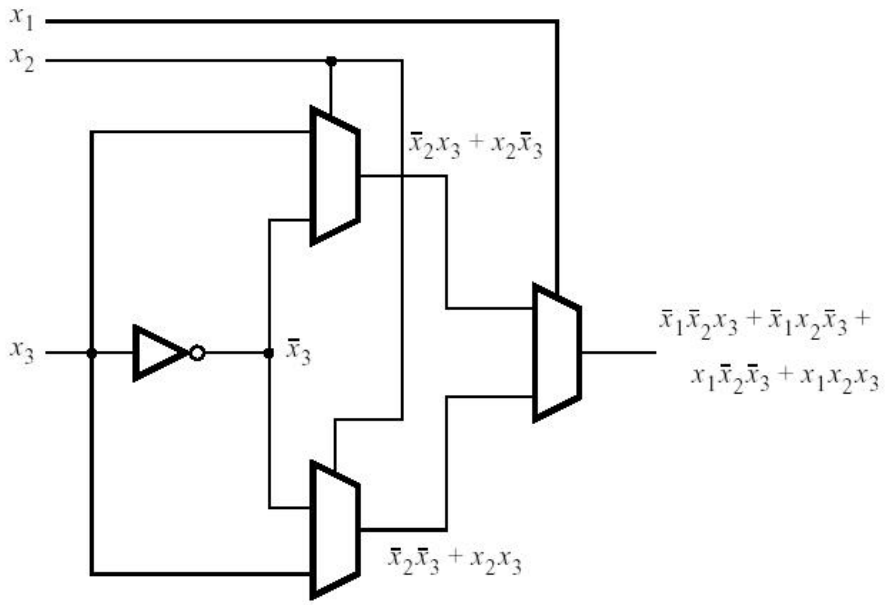
Chapter 3

3.1. (*a*)

x_1	x_2	x_3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(*b*) $$\#\text{transistors} = 48$$

3.2.



3.3. (*a*) $x_1\overline{x}_2\overline{x}_3 + \overline{x}_1x_2\overline{x}_3 + \overline{x}_1\overline{x}_2x_3 + x_1x_2x_3$

(b) $$\#\text{transistors} = 2 \times 8 = 16$$

3.4. The number of transistors needed is 16.

3.6. (*a*)

x_1	x_2	x_3	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

(*b*) #transistors $= 58$

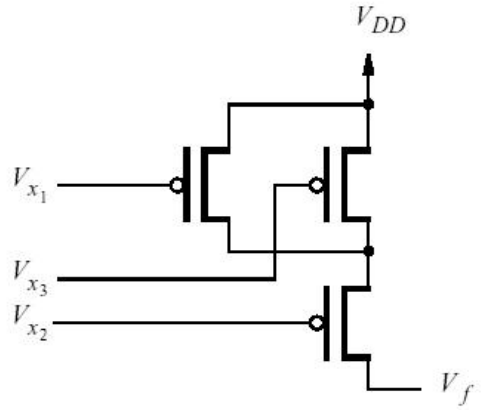
3.7. (*a*)

x_1	x_2	x_3	x_4	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

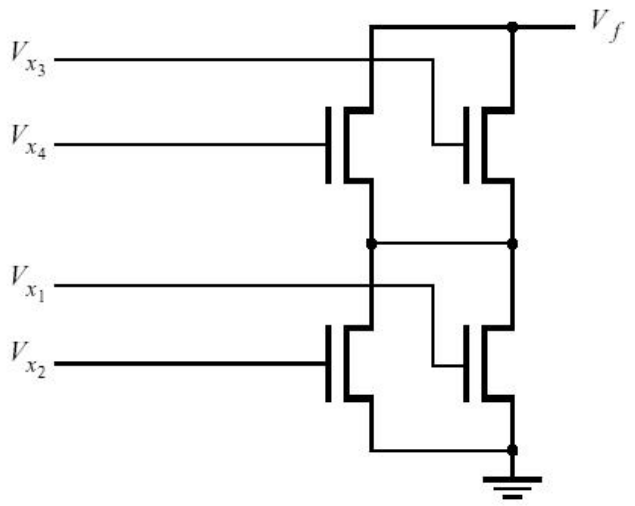
x_1	x_2	x_3	x_4	f
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

(*b*) #transistors $= 28$

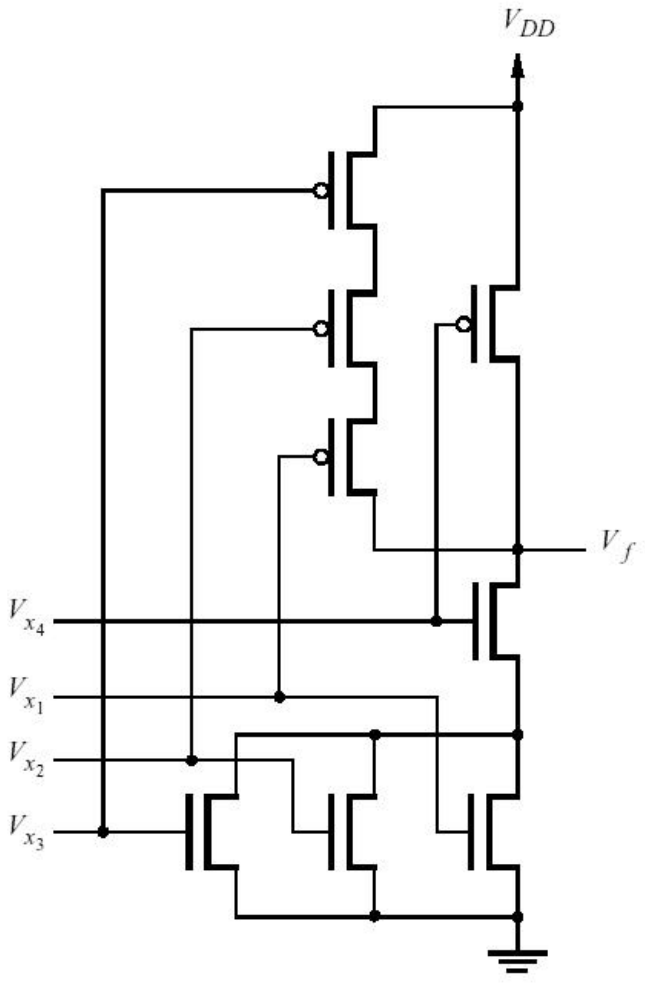
3.8.



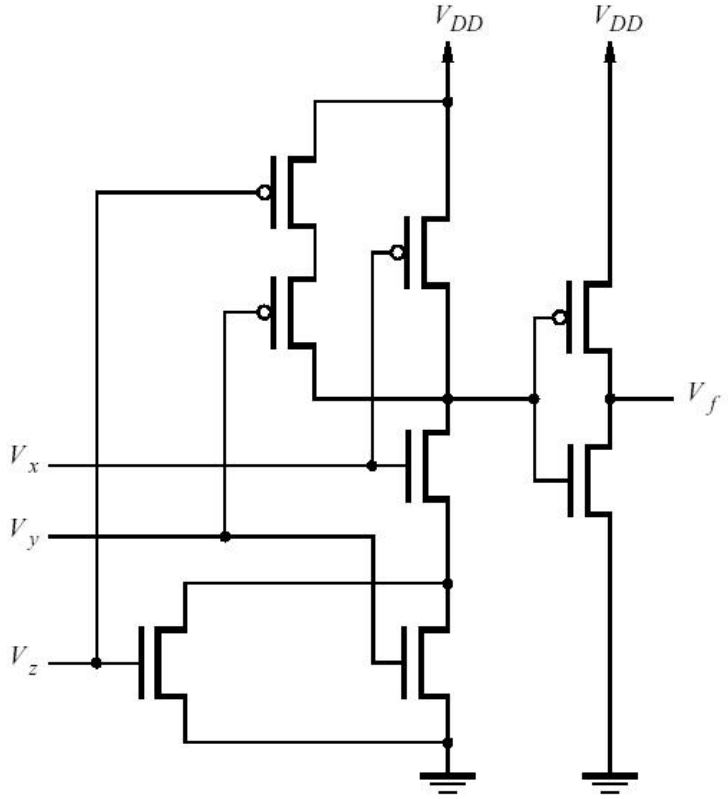
3.9.



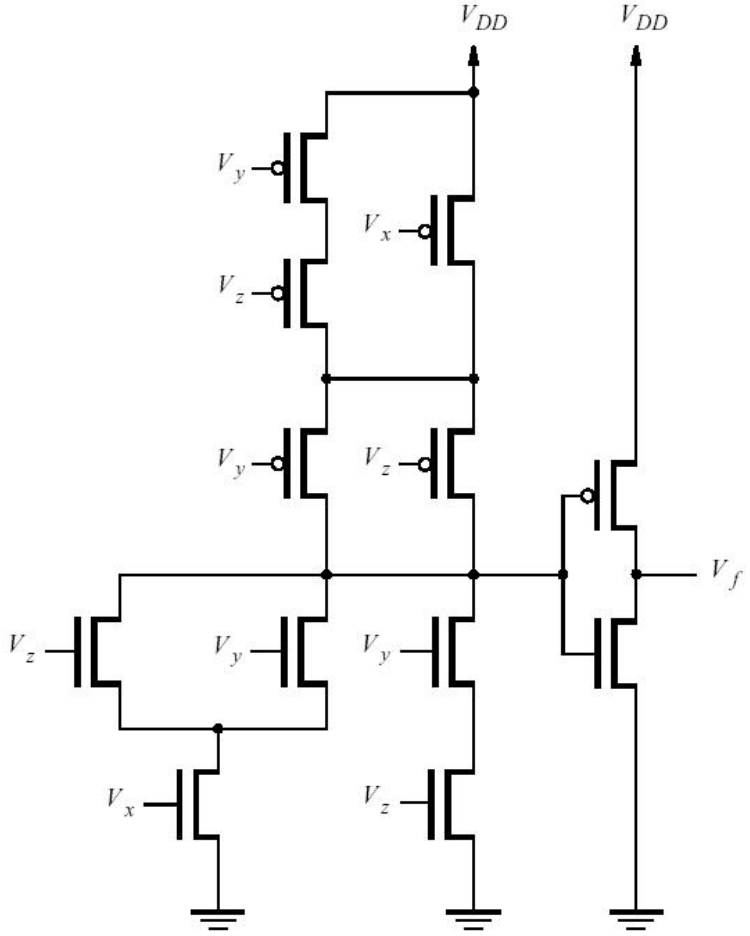
3.11.



3.12.



3.13.



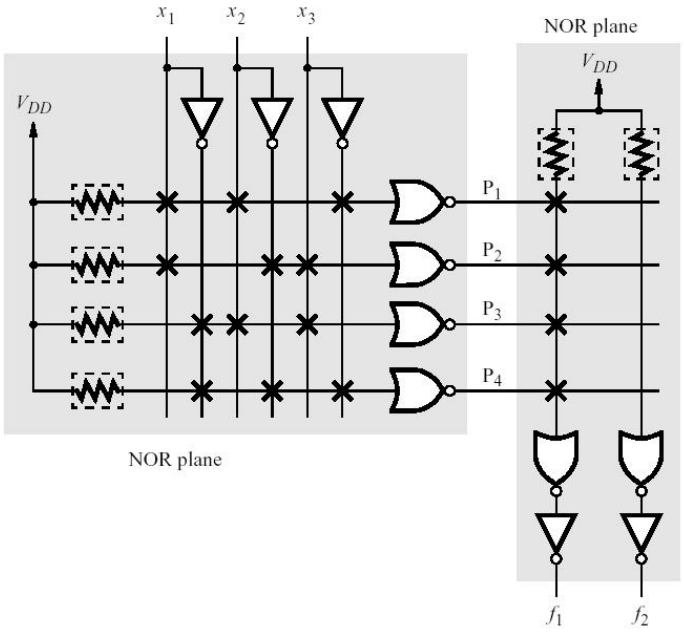
3.25. (*a*)

$$NM_H = 0.5\ \text{V}$$
$$NM_L = 0.7\ \text{V}$$

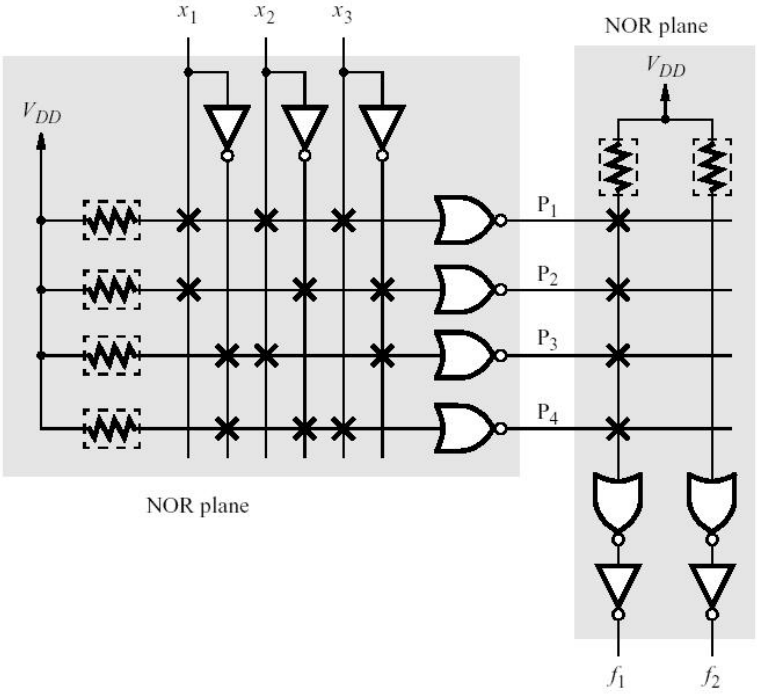
(*b*) $V_{OL} = 0.8\ \text{V}$

$$NM_L = 0.2\ \text{V}$$

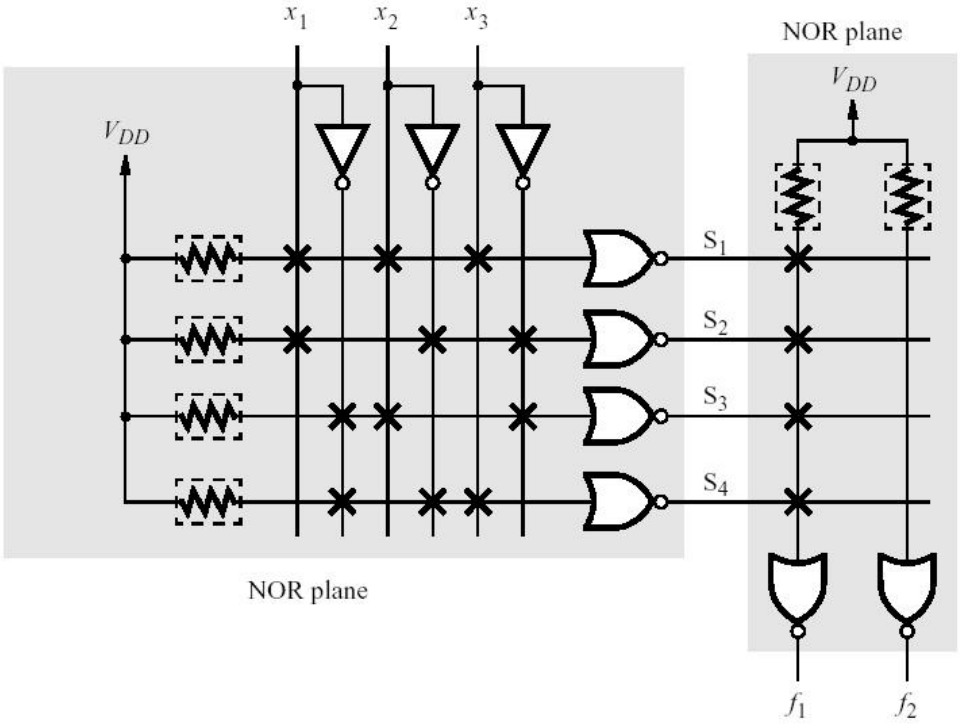
3.36.



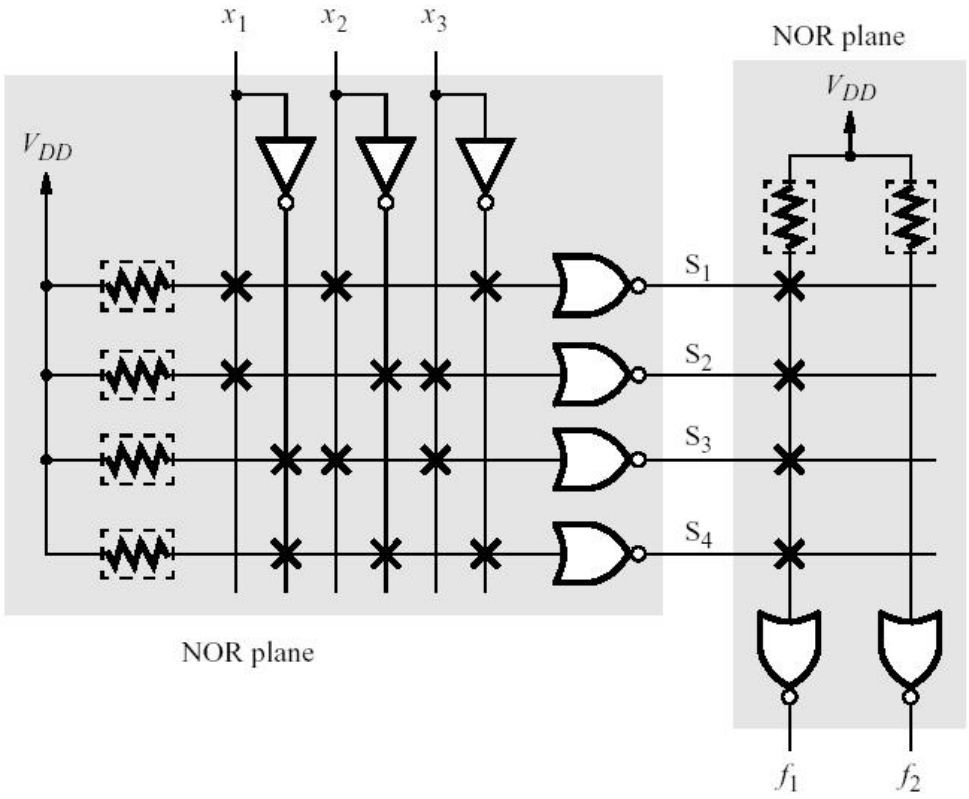
3.37.



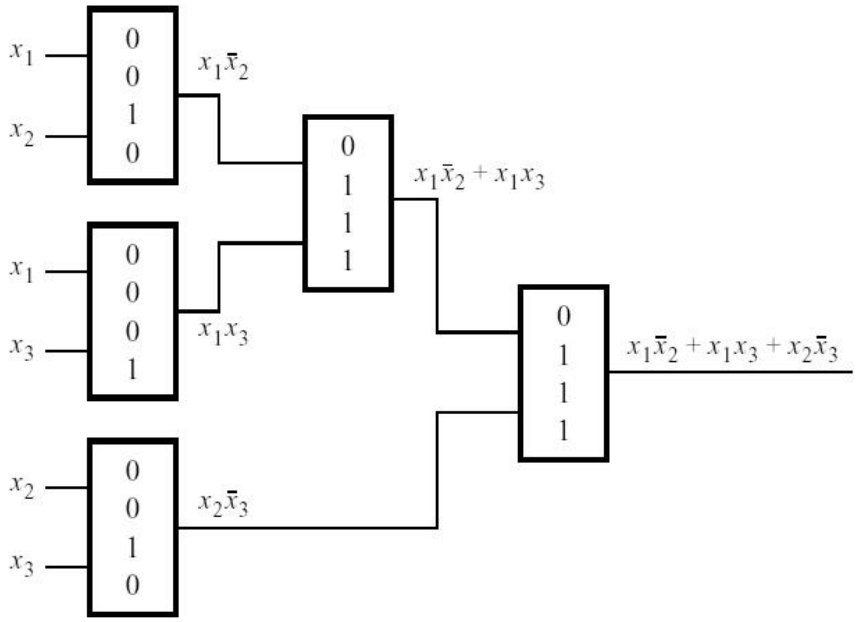
3.38.


x_1
x_2
x_3
NOR plane
V_{DD}
V_{DD}
S_1
S_2
S_3
S_4
NOR plane
f_1
f_2

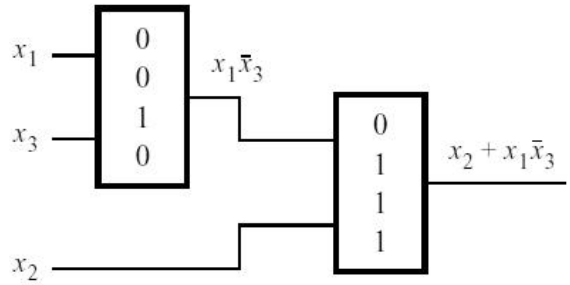
3.39.


x_1
x_2
x_3
NOR plane
V_{DD}
V_{DD}
S_1
S_2
S_3
S_4
NOR plane
f_1
f_2

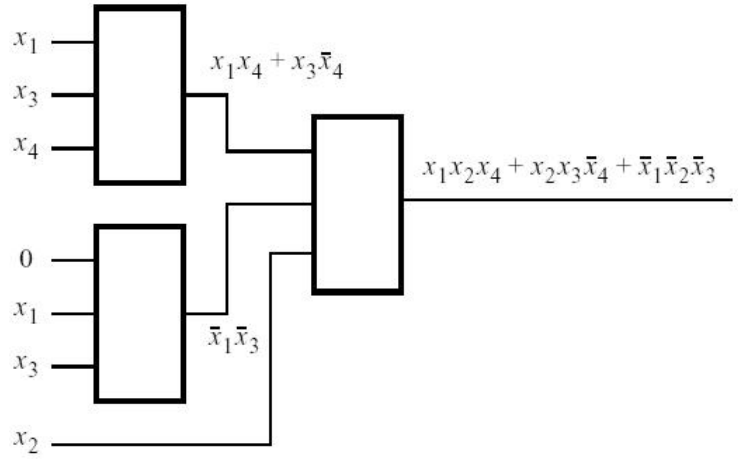
3.44.


x_1
x_2
0 0 1 0
$x_1\bar{x}_2$
x_1
x_3
0 0 0 1
x_1x_3
0 1 1 1
$x_1\bar{x}_2 + x_1x_3$
x_2
x_3
0 0 1 0
$x_2\bar{x}_3$
0 1 1 1
$x_1\bar{x}_2 + x_1x_3 + x_2\bar{x}_3$

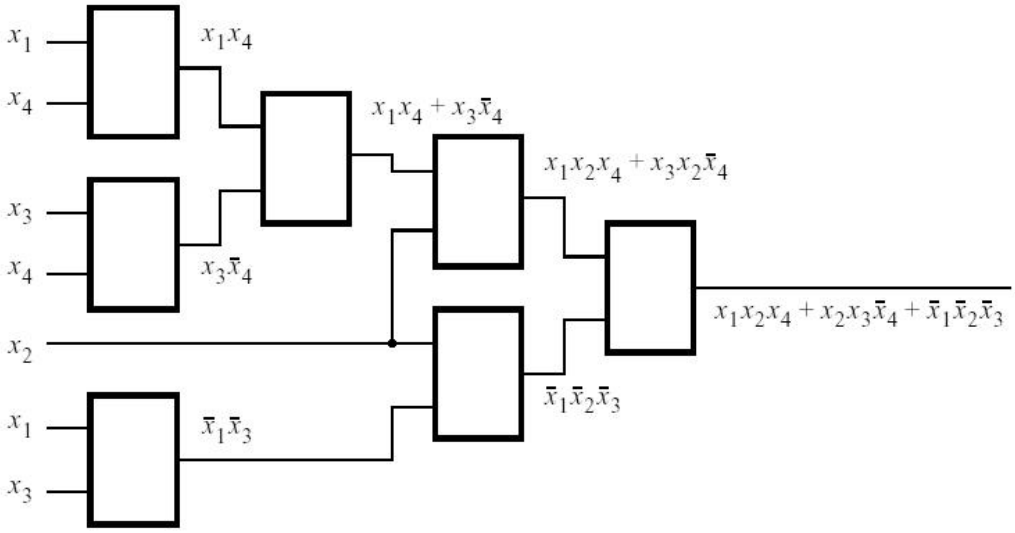
3.45.


x_1
x_3
0 0 1 0
$x_1\bar{x}_3$
x_2
0 1 1 1
$x_2 + x_1\bar{x}_3$

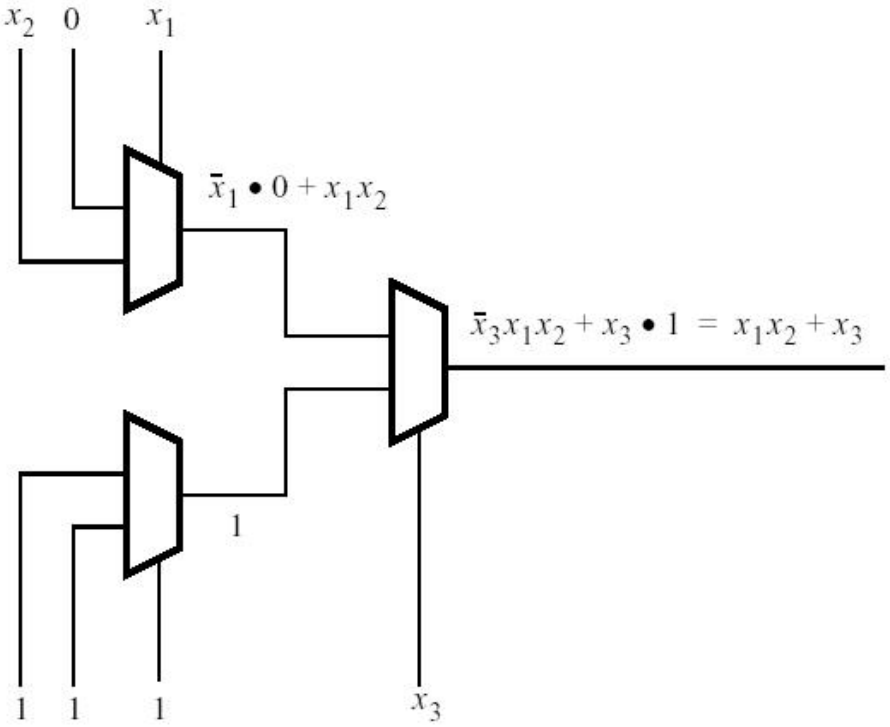
3.46.


x_1
x_3
x_4
$x_1x_4 + x_3\bar{x}_4$
0
x_1
x_3
$\bar{x}_1\bar{x}_3$
x_2
$x_1x_2x_4 + x_2x_3\bar{x}_4 + \bar{x}_1\bar{x}_2\bar{x}_3$

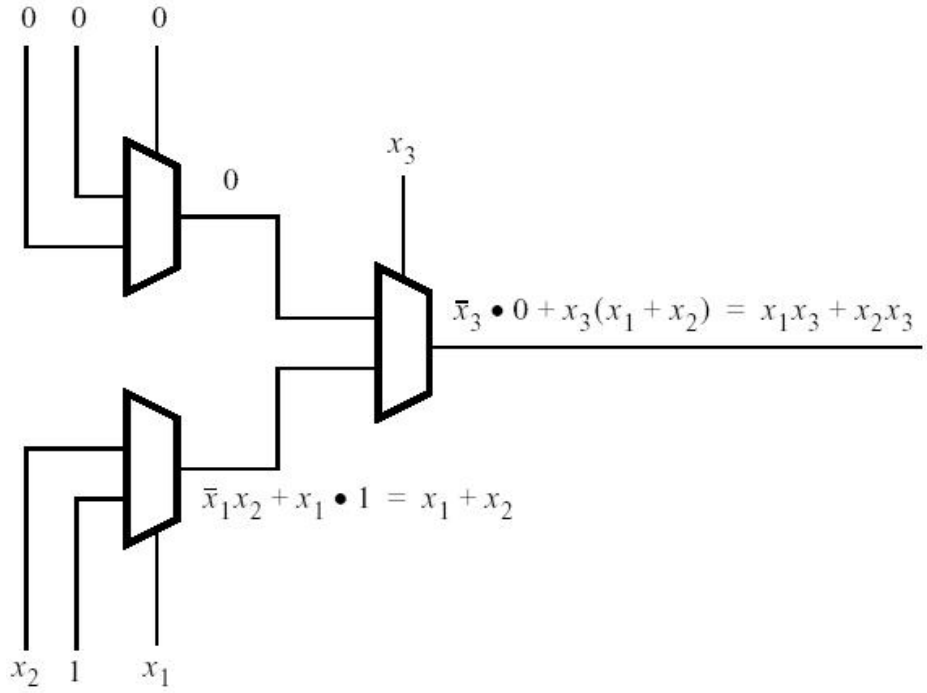
3.47.


x_1
x_4
x_1x_4
$x_1x_4 + x_3\bar{x}_4$
$x_1x_2x_4 + x_3x_2\bar{x}_4$
x_3
x_4
$x_3\bar{x}_4$
$x_1x_2x_4 + x_2x_3\bar{x}_4 + \bar{x}_1\bar{x}_2\bar{x}_3$
x_2
$\bar{x}_1\bar{x}_2\bar{x}_3$
x_1
x_3
$\bar{x}_1\bar{x}_3$

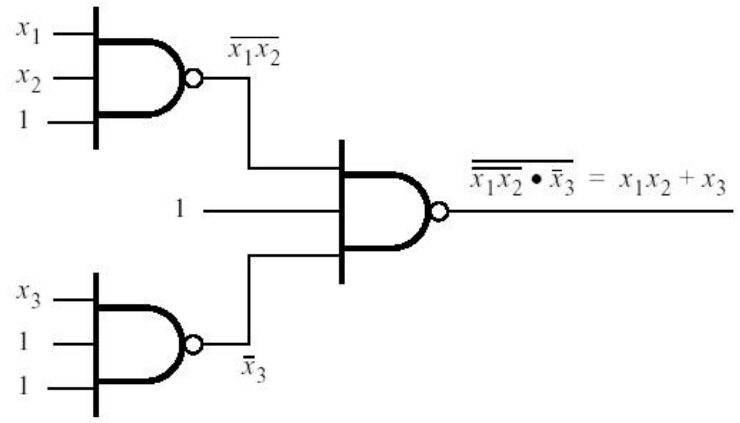
3.49. (*a*)


x_2 0 x_1
$\bar{x}_1 \bullet 0 + x_1x_2$
$\bar{x}_3x_1x_2 + x_3 \bullet 1 = x_1x_2 + x_3$
1
1 1 1
x_3

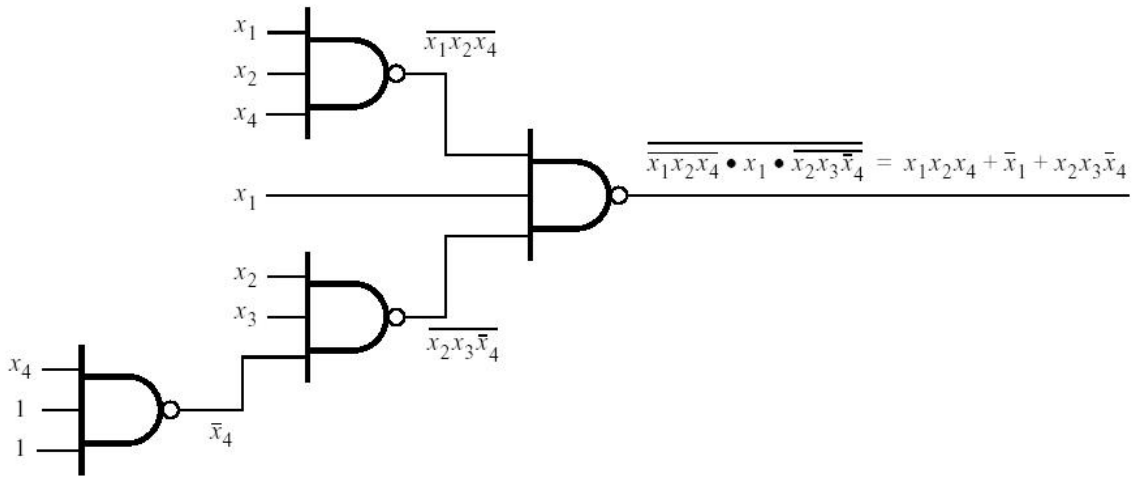
(*b*)


0 0 0
0
x_3
$\bar{x}_3 \bullet 0 + x_3(x_1 + x_2) = x_1x_3 + x_2x_3$
$\bar{x}_1x_2 + x_1 \bullet 1 = x_1 + x_2$
x_2 1 x_1

3.50. (*a*)


x_1
x_2
1
$\overline{x_1x_2}$
$\overline{\overline{x_1x_2} \bullet \bar{x}_3} = x_1x_2 + x_3$
1
x_3
1
1
$\bar{x}_3$

(*b*)


x_1
x_2
x_4
$\overline{x_1x_2x_4}$
$\overline{\overline{x_1x_2x_4} \bullet x_1 \bullet \overline{x_2x_3\bar{x}_4}} = x_1x_2x_4 + \bar{x}_1 + x_2x_3\bar{x}_4$
x_1
x_2
x_3
$\overline{x_2x_3\bar{x}_4}$
x_4
1
1
$\bar{x}_4$

3.51.

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY prob3_51 IS
    PORT ( x1, x2, x3, x4  : IN   STD_LOGIC ;
           f               : OUT  STD_LOGIC ) ;
END prob3_51 ;

ARCHITECTURE LogicFunc OF prob3_51 IS
BEGIN
    f <= (x2 AND NOT x3 AND NOT x4) OR
         (NOT x1 AND x2 AND x4) OR
         (NOT x1 AND x2 AND x3) OR (x1 AND x2 AND x3) ;
END LogicFunc ;
```

3.52.

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY prob3_52 IS
    PORT ( x1, x2, x3, x4  : IN   STD_LOGIC ;
           f               : OUT  STD_LOGIC ) ;
END prob3_52 ;

ARCHITECTURE LogicFunc OF prob3_52 IS
BEGIN
    f <= (x1 OR x2 OR NOT x4) AND
         (NOT x2 OR x3 OR NOT x4) AND
         (NOT x1 OR x3 OR NOT x4) AND
         (NOT x1 OR NOT x3 OR NOT x4) ;
END LogicFunc ;
```