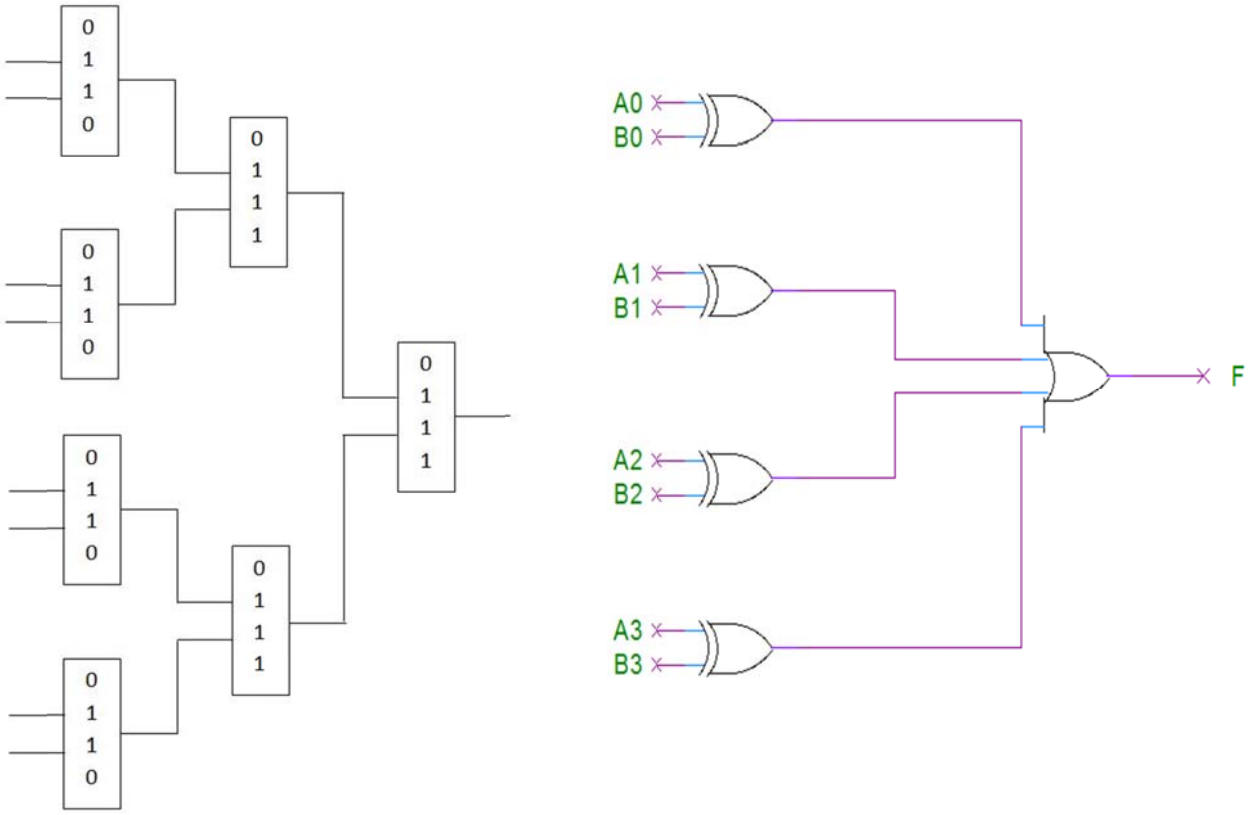
COE-328 Final Exam 2008

1. Design a comparator that compares a 4-bit number A to a 4-bit number B and gives an Output F=1 if A is not equal B. You must use 2-input LUTs only.



2. Given the following logic circuit, clock signal, and input waveforms:

a) Derive the state-assigned table

b) Sketch the waveforms for Q1, Q2, Y1, and Y2 in the space provided.

Note: Assume zero delay for all gates and flip-flops.

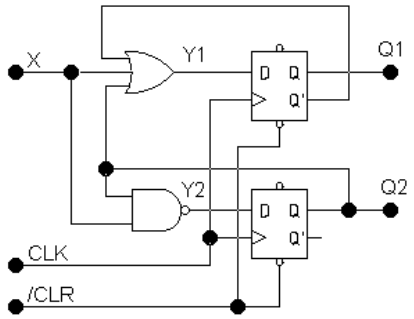


Figure 1

$$Y_1 = X + \overline{Q_1} + Q_2$$

$$Y_2 = \overline{X \cdot Q_2}$$

$Q_2\ Q_1$	X=0	X=1
	$Y_2\ Y_1$	$Y_2\ Y_1$
0 0	1 1	1 1
0 1	1 0	1 1
1 0	1 1	0 1
1 1	1 1	0 1

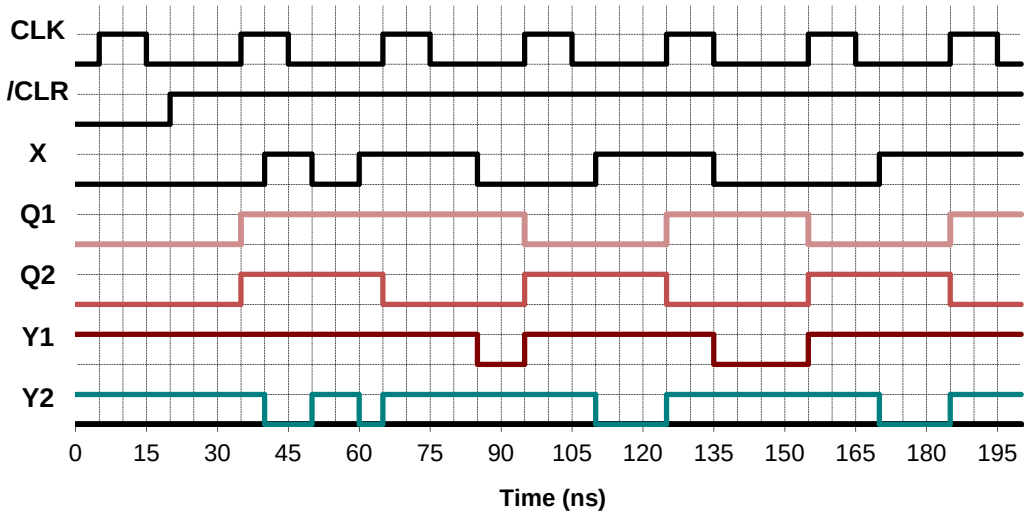
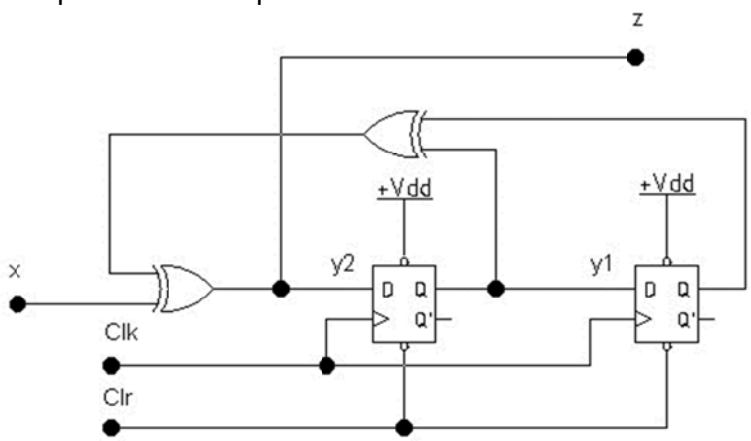


Figure 2

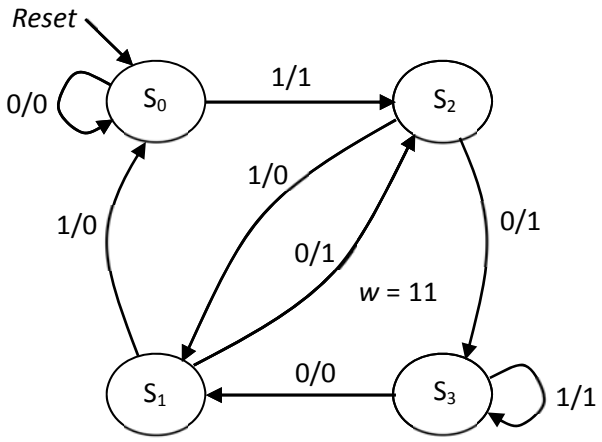
3. Given the following logic circuit, derive its state table and state diagram. If the following sequence 1010110101 is applied to the *x* input of the circuit with the initial sate 01, determine the resulting output sequence on *z* output.



$$y_1 = Q_2$$

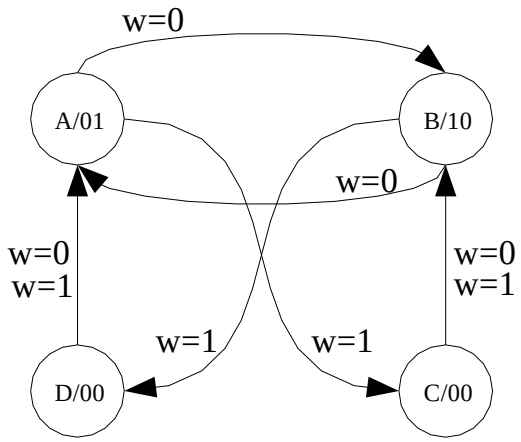
$$y_2 = x \oplus Q_1 \oplus Q_2$$

$Q_2\ Q_1$	x=0	x=1	x=0	x=1
	$y_2\ y_1$	$y_2\ y_1$	z	
0 0	0 0	1 0	0	1
0 1	1 0	0 0	1	0
1 0	1 1	0 1	1	0
1 1	0 1	1 1	0	1



S	S_1	S_0	S_0	S_2	S_3	S_3	S_3	S_1	S_0	S_0
x	1	0	1	0	1	1	0	1	0	1
$z=y_2$	0	0	1	1	1	1	0	0	0	1

4. The state diagram for a finite state machine (FSM) with one input *w* and two outputs *z2* and *z1* is given below



a) Does the above state diagram use a Moore or Mealy-type model to represent the FSM? Explain your answer.

The state diagram represents Moore-type FSM, since outputs are completely defined by states and do not depend on inputs.

b) What is the minimum number of state variables required to represent the states? Explain your answer.

Two state variables are required, because $2^2 = 4$, where 4 is the number of states.

c) Using the state assignment: A=00, B=01, C=11, and D=10, develop the next state and output equations for implementing the FSM.

	$Q_2\ Q_1$	w=0	w=1	$z_2\ z_1$
		$D_2\ D_1$	$D_2\ D_1$	
A	0 0	0 1	1 1	0 1
B	0 1	0 0	1 0	1 0
C	1 1	0 1	0 1	0 0
D	1 0	0 0	0 0	0 0

D_2

$w \setminus Q_2Q_1$	0 0	0 1	1 1	1 0
0	0	0	0	0
1	1	1	0	0

$$D_2 = \overline{Q_2}w$$

D_1

$w \setminus Q_2Q_1$	0 0	0 1	1 1	1 0
0	1	0	1	0
1	1	0	1	0

$$Y_1 = \overline{Q_2}\,\overline{Q_1} + Q_2Q_1$$

z_2

$Q_2 \setminus Q_1$	0	1
0	0	1
1	0	0

$$z_2 = \overline{Q_2}Q_1$$

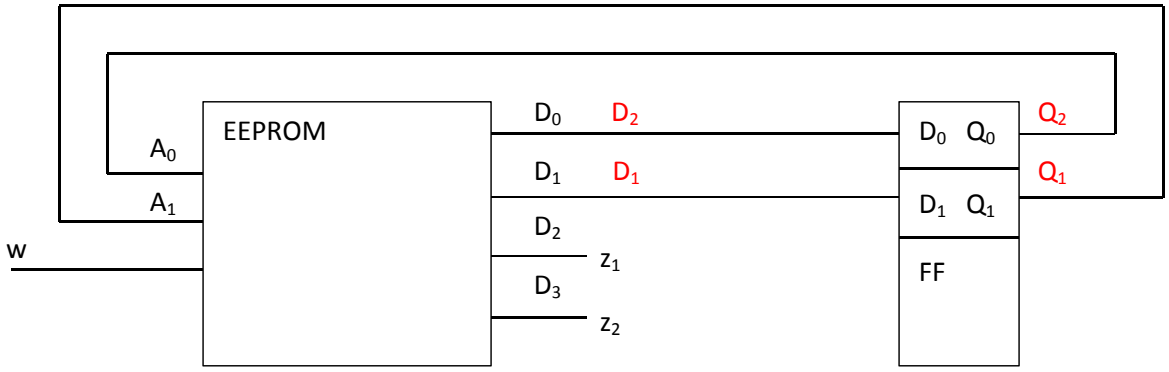
z_1

$Q_2 \setminus Q_1$	0	1
0	1	0
1	0	0

$$z_1 = \overline{Q_2}\,\overline{Q_1}$$

5. Assuming that an 8 x 4-bit EPROM is available, explain how the FSM can be implemented with the state assignment in Part C. Fill in the contents of the EPROM in the table below and clearly explain what the addresses and contents of the EPROM represent.

Content				Address
D_3	D_2	D_1	D_0	w A_2 A_1
0	1	1	0	0 0 0
1	0	0	0	0 0 1
0	0	0	0	0 1 0
0	0	1	0	0 1 1
0	1	1	1	1 0 0
1	0	0	1	1 0 1
0	0	0	0	1 1 0
0	0	1	0	1 1 1



	Q_2 Q_1	w=0	w=1	z_2 z_1
		D_2 D_1	D_2 D_1	
A	0 0	0 1	1 1	0 1
B	0 1	0 0	1 0	1 0
C	1 1	0 1	0 1	0 0
D	1 0	0 0	0 0	0 0

6. Which circuit does the following VHDL code represent?

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY system IS
     PORT (Clock, Reset : IN STD_logic;
          z           : OUT STD_LOGIC_VECTOR(2 DOWNTO 0));
END system;

ARCHITECTURE Behavior OF system IS
   TYPE State_type IS (A,B,C);
    SIGNAL y: State_type;
BEGIN
 PROCESS (Reset, Clock)
 BEGIN
     IF Reset='0' THEN
         y<=A;
     ELSIF(Clock'EVENT AND Clock='1') THEN
         CASE y IS
           WHEN A=>  THEN y<=B;
           WHEN B=>  THEN y<=C;
           WHEN C=>  THEN y<=A;
         END CASE;
     END IF;
  END PROCESS;
 PROCESS(y)
 BEGIN
    CASE y IS
        WHEN A=>
           z <= "110";
        WHEN B=>
           z <= "101";
        WHEN C=>
           z <= "011";
    END CASE;
  END PROCESS;
END Behavior;
```