Chapter 8

8.1. The expressions for the inputs of the flip-flops are

$$\begin{aligned} D_2 &= Y_2 = \overline{w}y_2 + \overline{y}_1\overline{y}_2 \\ D_1 &= Y_1 = w \oplus y_1 \oplus y_2 \end{aligned}$$

The output equation is

$$z = y_1 y_2$$

8.2.

The expressions for the inputs of the flip-flops are

$$\begin{aligned} J_2 &= \overline{y}_1 \\ K_2 &= w \\ J_1 &= \overline{w}y_2 + w\overline{y}_2 \\ K_1 &= J_1 \end{aligned}$$

The output equation is

$$z = y_1 y_2$$

8.3. A possible state table is

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	E	C	0	0
C	E	D	0	0
D	E	D	0	1
E	F	B	0	0
F	A	B	0	1

8.7. For Figure 8.51

$$
\begin{aligned}
Y_3 &= \overline{w}y_3 + \overline{y}_1y_2 + wy_1\overline{y}_3 \\
Y_2 &= wy_3 + w\overline{y}_1\overline{y}_2 + wy_1y_2 + \overline{w}y_1\overline{y}_2\overline{y}_3 \\
Y_1 &= \overline{y}_3\overline{w} + \overline{y}_1\overline{w} + wy_1\overline{y}_2 \\
z &= y_1\overline{y}_3 + \overline{y}_2\overline{y}_3
\end{aligned}
$$

For Figure 8.52

$$
\begin{aligned}
Y_2 &= \overline{w}y_2 + \overline{y}_1y_2 + w\overline{y}_2 \\
Y_1 &= \overline{y}_1\overline{w} + wy_1\overline{y}_2 \\
z &= \overline{y}_2
\end{aligned}
$$

8.8. For Figure 8.55

$$
\begin{aligned}
Y_4 &= Dy_3 \\
Y_3 &= Dy_1 + Dy_2 + Ny_2 + \overline{D}y_3\overline{y}_2y_1 \\
Y_2 &= N\overline{y}_2 + y_3\overline{y}_1 + \overline{N}\overline{y}_3y_2\overline{y}_1 \\
Y_1 &= Ny_2 + D\overline{y}_2\overline{y}_1 + \overline{D}\overline{y}_2y_1 \\
z &= y_4 + y_1y_2 + \overline{y}_1y_3
\end{aligned}
$$

for Figure 8.56

$$
\begin{aligned}
Y_3 &= D\overline{y}_2y_1 \\
Y_2 &= y_3 + \overline{N}y_2\overline{y}_1 + N\overline{y}_2 \\
Y_1 &= \overline{D}\overline{y}_2y_1 + Ny_2\overline{y}_1 + D\overline{y}_3\overline{y}_1 \\
z &= y_3 + y_2y_1
\end{aligned}
$$

8.9.

$$
\begin{aligned}
Y_2 &= \overline{k}y_1 + \overline{k}y_2 \\
Y_1 &= \overline{k}\overline{y}_1 + \overline{k}y_2 \\
z &= \overline{k}y_1y_2
\end{aligned}
$$

8.10.

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY prob8_10 IS
    PORT ( Clock    : IN    STD_LOGIC ;
           Resetn   : IN    STD_LOGIC ;
           w1, w2   : IN    STD_LOGIC ;
           z        : OUT   STD_LOGIC) ;
END prob8_10 ;

ARCHITECTURE Behavior OF prob8_10 IS
    TYPE State_type IS ( A, B, C, D ) ;
    SIGNAL y : State_type ;
    SIGNAL k : STD_LOGIC ;
 BEGIN
     k <= w1 XOR w2 ;
     PROCESS ( Resetn, Clock )
     BEGIN
         IF Resetn = '0' THEN
             y <= A ;
         ELSIF (Clock'EVENT AND Clock = '1') THEN
             CASE y IS
                 WHEN A =>
                     IF k = '0' THEN y <= B ;
                     ELSE y <= A ;
                     END IF ;
                 WHEN B =>
                     IF k = '0' THEN y <= C ;
                     ELSE y <= A ;
                     END IF ;
                 WHEN C =>
                     IF k = '0' THEN y <= D ;
                     ELSE y <= A ;
                     END IF ;
                 WHEN D =>
                     IF k = '0' THEN y <= D ;
                     ELSE y <= A ;
                     END IF ;
             END CASE ;
         END IF ;
     END PROCESS ;

     z <= '1' WHEN y = D AND k = '0' ELSE '0' ;
 END Behavior ;
```

8.15.

The next-state expressions are

$$\begin{aligned} D_4 &= Y_4 = \overline{w}y_3 + wy_1 \\ D_3 &= Y_3 = \overline{w}(y_1 + y_4) \\ D_2 &= Y_2 = \overline{w}y_2 + wy_4 \\ D_1 &= Y_1 = w(y_2 + y_1) \end{aligned}$$

The output is given by $z = y_4$.

8.19.

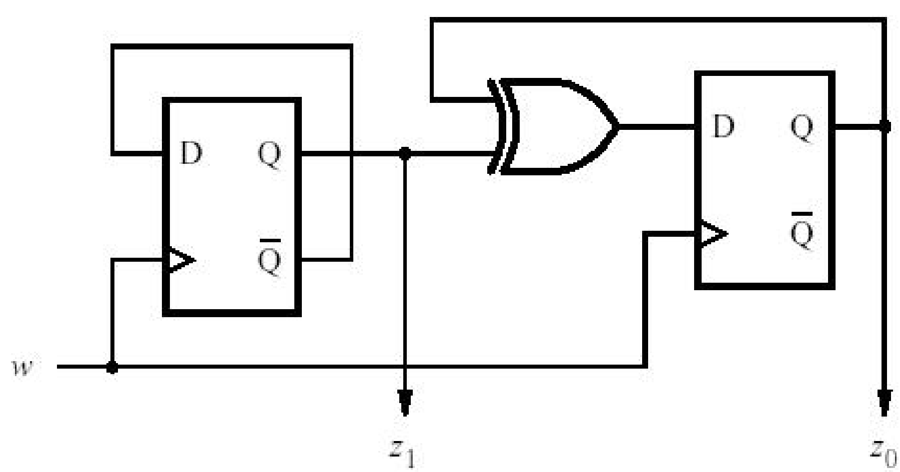
$$\begin{aligned} Y_2 &= Dy_1 + \overline{D}y_2\overline{N} + N\overline{y}_2\overline{y}_1 \\ Y_1 &= Ny_2 + \overline{D}y_1\overline{N} + D\overline{y}_2\overline{y}_1 \\ z &= Dy_1 + Dy_2 + Ny_1 \end{aligned}$$

8.20.

The next-state expressions are

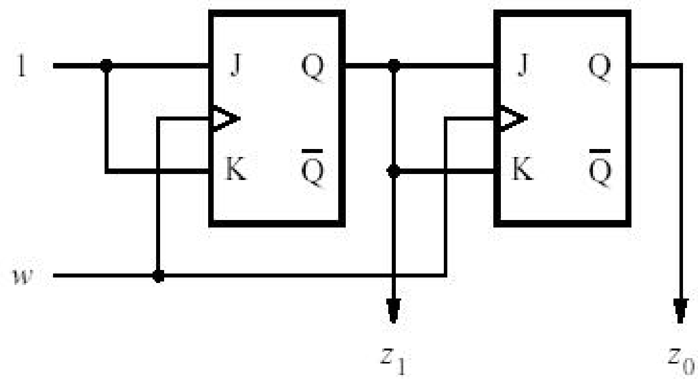
$$\begin{aligned} Y_1 &= \overline{y}_1 \\ Y_2 &= y_1 \oplus y_2 \end{aligned}$$

The resulting circuit is



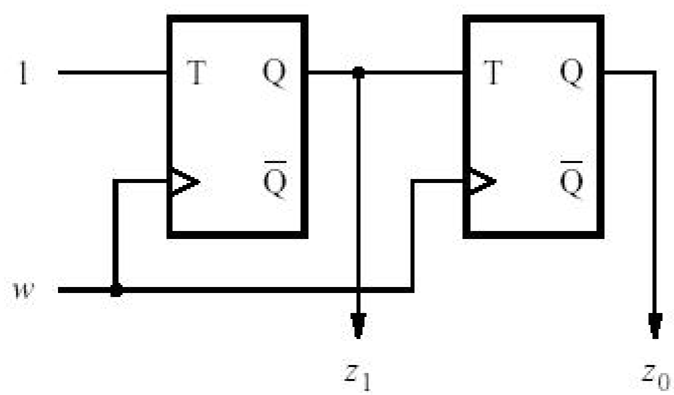
8.21.

The flip-flop inputs are $J_1 = K_1 = 1$ and $J_2 = K_2 = y_1$. The resulting circuit is



8.22.

The flip-flop inputs are $T_1 = 1$ and $T_2 = y_1$. The resulting circuit is



8.23.

The next-state expressions are

$$
\begin{aligned}
Y_2 &= \overline{y}_0 y_2 + \overline{w} y_2 + w y_0 y_1 \\
Y_1 &= \overline{y}_0 y_1 + \overline{w} y_1 + w y_0 \overline{y}_1 \overline{y}_2 \\
Y_0 &= \overline{w} y_0 + w \overline{y}_0
\end{aligned}
$$

The outputs are: $z_2 = y_2$, $z_1 = y_1$, and $z_0 = y_0$.

8.24.

The expressions for the inputs of the flip-flops are

$$\begin{aligned} J_2 &= wy_1y_0 \\ K_2 &= wy_2y_0 \\ J_1 &= w\overline{y}_2y_0 \\ K_1 &= wy_0 \\ J_0 &= w \\ K_0 &= w \end{aligned}$$

The outputs are: $z_2 = y_2$, $z_1 = y_1$, and $z_0 = y_0$.

8.25.

The expressions for T inputs of the flip-flops are

$$\begin{aligned} T_2 &= wy_1y_0 + wy_2y_0 \\ T_1 &= w\overline{y}_2y_0 \\ T_0 &= w \end{aligned}$$

The outputs are: $z_2 = y_2$, $z_1 = y_1$, and $z_0 = y_0$.

8.26.

The next-state expressions (inputs to D flip-flops) are

$$\begin{aligned} D_2 &= Y_2 &&= w\overline{y}_2y_1 + \overline{w}y_2y_1 + wy_2\overline{y}_1 + \overline{w}y_2y_0 + \overline{y}_2\overline{y}_1\overline{y}_0w \\ D_1 &= Y_1 &&= w\overline{y}_1 + \overline{y}_1\overline{y}_0 + \overline{w}y_1y_0 \\ D_0 &= Y_0 &&= \overline{y}_0\overline{w} + y_0w \end{aligned}$$

The outputs are: $z_2 = y_2$, $z_1 = y_1$, and $z_0 = y_0$.

8.27.
The expressions for J and K inputs to the three flip-flops are

$$\begin{aligned} J_2 &= y_1 w + \overline{y}_1 \overline{y}_0 \overline{w} \\ K_2 &= J_2 \\ J_1 &= w + \overline{y}_0 \\ K_1 &= J_1 \\ J_0 &= \overline{w} \\ K_0 &= J_0 \end{aligned}$$

The outputs are: $z_2 = y_2$, $z_1 = y_1$, and $z_0 = y_0$.

8.28.
The expressions for T inputs of the flip-flops are

$$\begin{aligned} T_2 &= \overline{y}_1 \overline{y}_0 \overline{w} + y_1 w \\ T_1 &= w + \overline{y}_0 \\ T_0 &= \overline{w} \end{aligned}$$

The outputs are: $z_2 = y_2$, $z_1 = y_1$, and $z_0 = y_0$.

8.29.

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	A	C	0
B	A	D	1
C	A	D	0
D	A	B	0

The circuit produces $z = 1$ whenever the input sequence on w comprises a 0 followed by an even number of 1s.