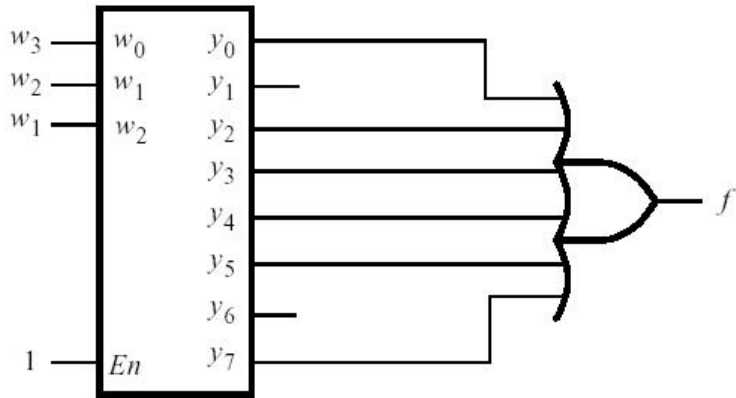
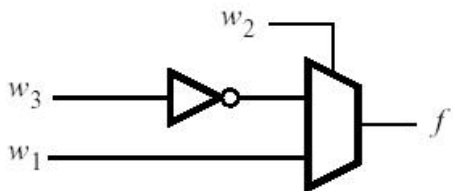


Chapter 6

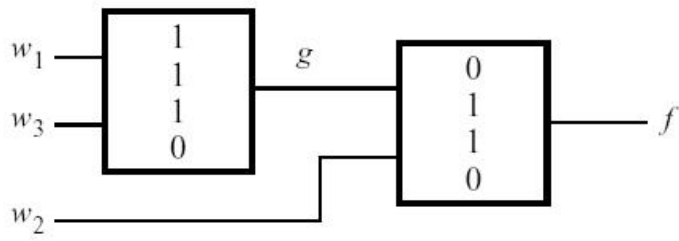
6.1.



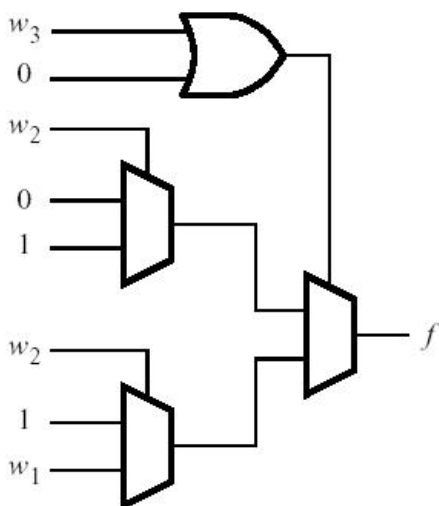
6.6.



6.11.



6.16.



6.18. The code in Figure P6.2 is a 2-to-4 decoder with an enable input.

```
6.19.      LIBRARY ieee ;
           USE ieee.std_logic-1164.all ;

           ENTITY prob6_19 IS
               PORT ( w : IN    STD_LOGIC_VECTOR(1 TO 3) ;
                     f : OUT STD_LOGIC ) ;
           END prob6_19 ;

           ARCHITECTURE Behavior OF prob6_19 IS
           BEGIN
               WITH w SELECT
                   f <= '0' WHEN "001",
                      '0' WHEN "110",
                      '1' WHEN OTHERS ;
           END Behavior ;

6.21.      LIBRARY ieee ;
           USE ieee.std_logic-1164.all ;

           ENTITY prob6_21 IS
               PORT ( w : IN    STD_LOGIC_VECTOR(3 DOWNT0 0) ;
                     y : OUT STD_LOGIC_VECTOR(1 DOWNT0 0) ) ;
           END prob6_21 ;

           ARCHITECTURE Behavior OF prob6_21 IS
           BEGIN
               WITH w SELECT
                   y <= "00" WHEN "0001",
                      "01" WHEN "0010",
                      "10" WHEN "0100",
                      "11" WHEN OTHERS ;
           END Behavior ;
```

6.24.

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY prob6_24 IS
    PORT ( w : IN  STD_LOGIC_VECTOR(7 DOWNTO 0) ;
          y : OUT STD_LOGIC_VECTOR(2 DOWNTO 0) ;
          z : OUT STD_LOGIC ) ;
END prob6_24 ;

ARCHITECTURE Behavior OF prob6_24 IS
BEGIN
    y <= "111" WHEN w(7) = '1' ELSE
        "110" WHEN w(6) = '1' ELSE
        "101" WHEN w(5) = '1' ELSE
        "100" WHEN w(4) = '1' ELSE
        "011" WHEN w(3) = '1' ELSE
        "010" WHEN w(2) = '1' ELSE
        "001" WHEN w(1) = '1' ELSE
        "000" ;
    z <= '0' WHEN w="00000000" ELSE '1' ;
END Behavior ;
```

6.25.

```
LIBRARY ieee ;
USE ieee.std_logic-1164.all ;

ENTITY prob6_25 IS
    PORT ( w : IN    STD_LOGIC_VECTOR(7 DOWNTO 0) ;
          y : OUT STD_LOGIC_VECTOR(2 DOWNTO 0) ;
          z : OUT STD_LOGIC ) ;
END prob6_25 ;

ARCHITECTURE Behavior OF prob6_25 IS
BEGIN
    PROCESS ( w )
    BEGIN
        IF w(7) = '1' THEN
            y <= "111" ;
        ELSIF w(6) = '1' THEN
            y <= "110" ;
        ELSIF w(5) = '1' THEN
            y <= "101" ;
        ELSIF w(4) = '1' THEN
            y <= "100" ;
        ELSIF w(3) = '1' THEN
            y <= "011" ;
        ELSIF w(2) = '1' THEN
            y <= "010" ;
        ELSIF w(1) = '1' THEN
            y <= "001" ;
        ELSE
            y <= "000" ;
        END IF ;
        IF w = "00000000" THEN
            z <= '0' ;
        ELSE
            z <= '1' ;
        END IF ;
    END PROCESS ;
END Behavior ;
```

```

6.28.      LIBRARY ieee ;
           USE ieee.std_logic_1164.all ;

           ENTITY prob6_28 IS
               PORT ( s   : IN    STD_LOGIC_VECTOR( 1 DOWNTO 0 ) ;
                     w   : IN    STD_LOGIC_VECTOR( 3 DOWNTO 0 ) ;
                     f   : OUT   STD_LOGIC ) ;
           END prob6_28 ;

ARCHITECTURE Structure OF prob6_28 IS
    COMPONENT dec2to4
        PORT ( w   : IN    STD_LOGIC_VECTOR(1 DOWNTO 0) ;
              En  : IN    STD_LOGIC ;
              y   : OUT   STD_LOGIC_VECTOR(0 TO 3) );
    END COMPONENT;
    SIGNAL High : STD_LOGIC ;
    SIGNAL y : STD_LOGIC_VECTOR( 3 DOWNTO 0 ) ;
BEGIN
    High <= '1' ;
    decoder: dec2to4 PORT MAP ( s, High, y ) ;
    f <= (w(0) AND y(0)) OR (w(1) AND y(1)) OR
        (w(2) AND y(2)) OR w(3) AND y(3) ) ;
END Structure ;

```

```

6.30.    LIBRARY ieee ;
          USE ieee.std_logic-1164.all ;

          ENTITY prob6_30 IS
              PORT ( bcd : IN    STD_LOGIC_VECTOR(3 DOWNTO 0) ;
                    leds : OUT  STD_LOGIC_VECTOR(1 TO 7) ) ;
          END prob6_30 ;

          ARCHITECTURE Behavior OF prob6_30 IS
          BEGIN
              WITH bcd SELECT
                  --      abcdefg
                  leds <= "1111110" WHEN "0000",
                        "0110000" WHEN "0001",
                        "1101101" WHEN "0010",
                        "1111001" WHEN "0011",
                        "0110011" WHEN "0100",
                        "1011011" WHEN "0101",
                        "1011111" WHEN "0110",
                        "1110000" WHEN "0111",
                        "1111111" WHEN "1000",
                        "1111011" WHEN "1001",
                        "-----" WHEN OTHERS ;
          END Behavior ;

```

6.31.

$$\begin{aligned}
 a &= w_3 + w_2 w_0 + w_1 + \overline{w_2} \overline{w_0} \\
 b &= w_3 + \overline{w_1} \overline{w_0} + w_1 w_0 + \overline{w_2} \\
 c &= w_2 + \overline{w_1} + w_0
 \end{aligned}$$