Chapter 2

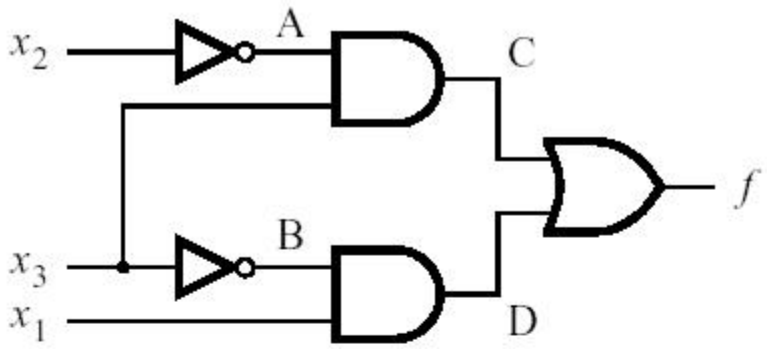
2.1. $x + yz$

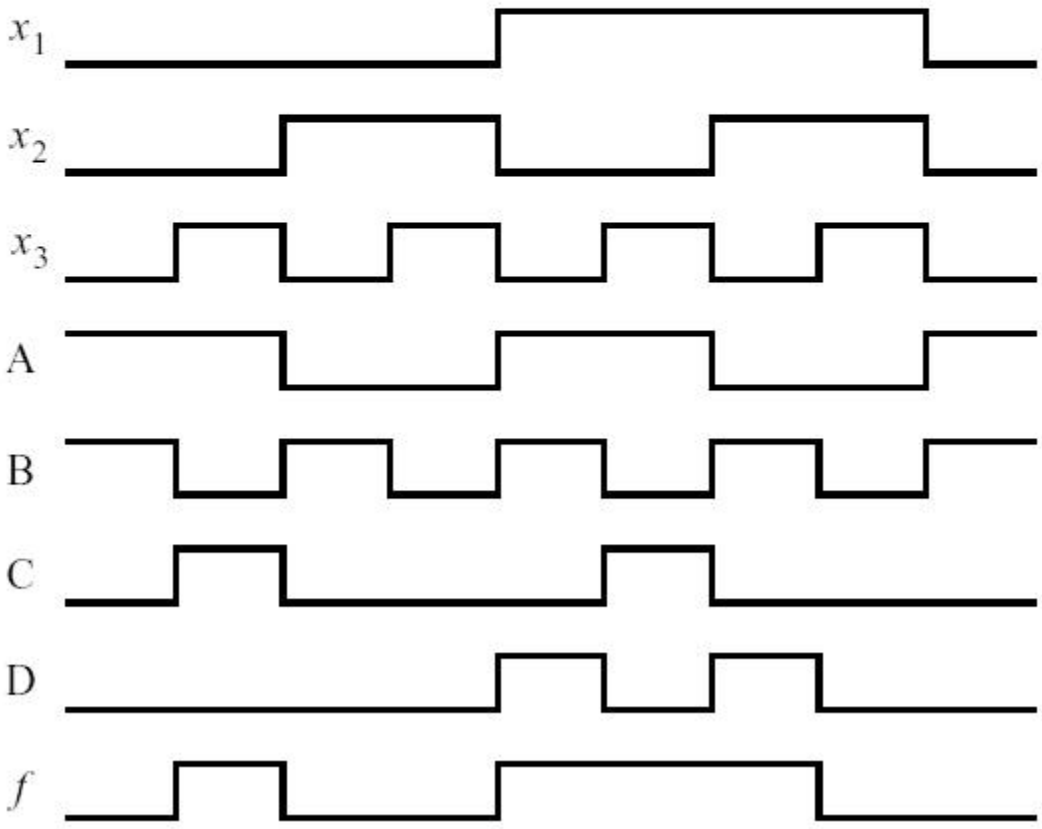
2.2. x

2.6.

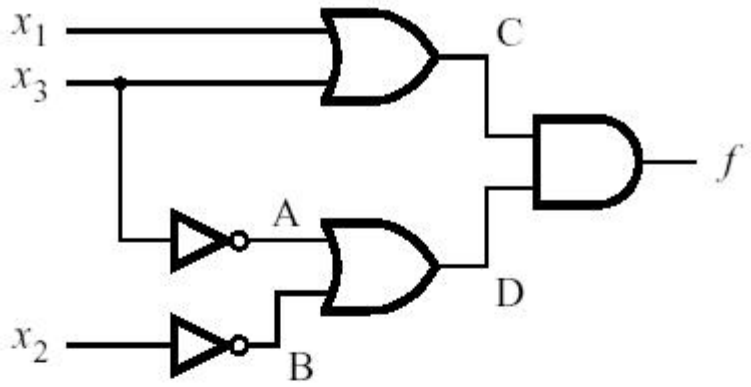
(a) Yes
(b) Yes
(c) No

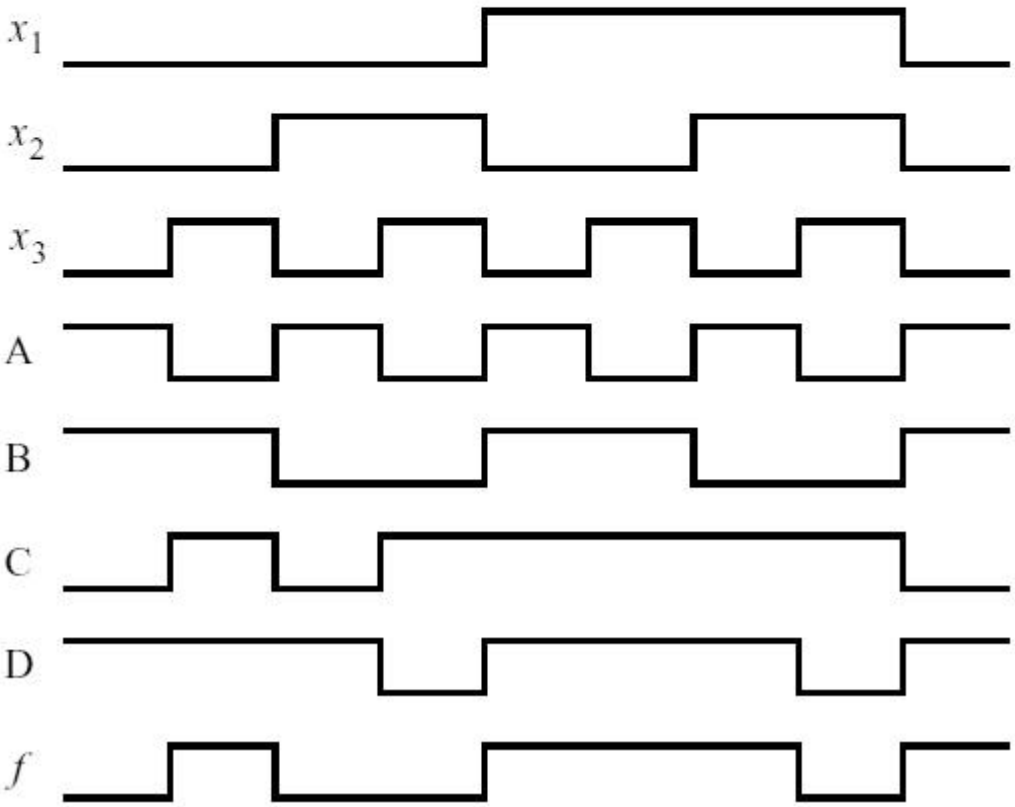
2.7.





2.8.





2.9. $x_1 + x_2 + x_3$

2.10. $x_1 x_2 x_3$

2.11. $x_1 x_3 + x_2 x_3 + \overline{x}_2 \overline{x}_3$

2.12. $x_1 \overline{x}_2 \overline{x}_3 + x_1 \overline{x}_2 \overline{x}_4 + x_1 x_2 x_4$

2.14. $(x_1 + x_2)(\overline{x}_2 + x_3)$

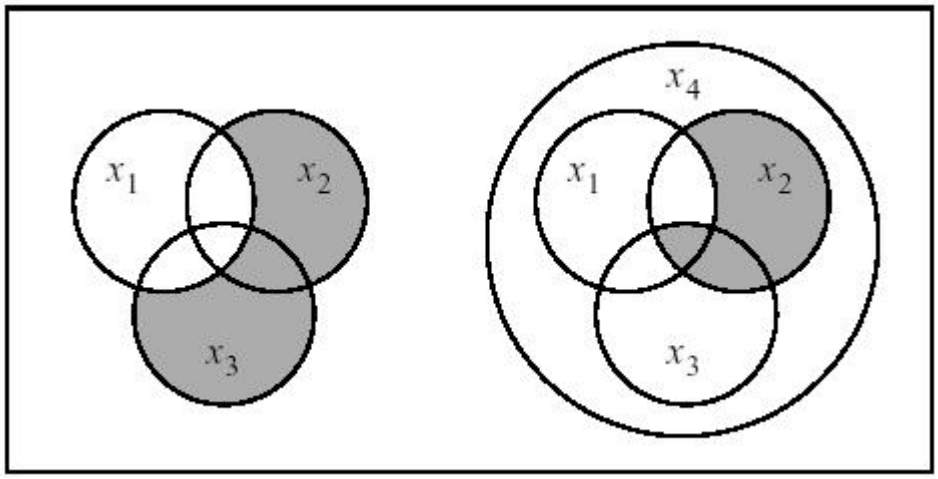
2.17. In Figure P2.1*a* it is impossible to represent the minterms

$$\overline{x}_1\overline{x}_2x_3x_4 \text{ and } x_1x_2\overline{x}_3\overline{x}_4.$$

In Figure P2.1*b*, it is impossible to represent the minterms

$$x_1x_2\overline{x}_3\overline{x}_4 \text{ and } x_1x_2x_3\overline{x}_4.$$

2.18.



2.19. $x_2x_3 + x_1\overline{x}_3$

2.20.

$$\overline{x}_1x_3 + x_1\overline{x}_3 + x_2x_3$$

Another possibility is $\overline{x}_1x_3 + x_1\overline{x}_3 + x_1x_2$

2.21.

$$(x_1 + x_3)(\overline{x}_1 + x_2 + \overline{x}_3)$$

2.22.

$$(x_1 + x_2)(\overline{x}_1 + \overline{x}_3)$$

2.25.

$$\overline{x}_1x_3 + \overline{x}_1x_2 + x_2x_3 + x_1\overline{x}_2\overline{x}_3$$

2.30.

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY prob2_30 IS
    PORT ( x1, x2, x3, x4   : IN     STD_LOGIC ;
           f1, f2           : OUT  STD_LOGIC ) ;
END prob2_30 ;

ARCHITECTURE LogicFunc OF prob2_30 IS
BEGIN
    f1 <= (x1 AND NOT x3) OR (x2 AND NOT x3) OR
          NOT x3 AND NOT x4) OR (x1 AND x2) OR
          x1 AND NOT x4) ;
    f2 <= (x1 OR NOT x3) AND (x1 OR x2 OR NOT x4) AND
          x2 OR NOT x3 OR NOT x4) ;
END LogicFunc ;
```

2.31.

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY prob2_31 IS
    PORT ( x1, x2, x3, x4   : IN     STD_LOGIC ;
           f1, f2           : OUT  STD_LOGIC ) ;
END prob2_31 ;

ARCHITECTURE LogicFunc OF prob2_31 IS
BEGIN
    f1 <= ((x1 AND x3) OR (NOT x1 AND NOT x3)) OR
          ((x2 AND x4) OR (NOT x2 AND NOT x4)) ;
    f2 <= (x1 AND x2 AND NOT x3 AND NOT x4) OR
          (NOT x1 AND NOT x2 AND x3 AND x4) OR
          (x1 AND NOT x2 AND NOT x3 AND x4) OR
          (NOT x1 AND x2 AND x3 AND NOT x4);
END LogicFunc ;
```