High-Power Converters and AC Drives

IEEE PESC2005 Tutorial

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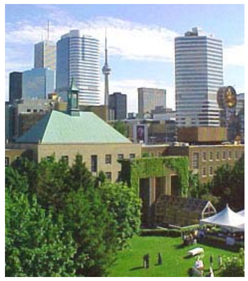


Ryerson Campus

Main Topics

1. Introduction
2. Cascaded H-Bridge Multilevel Inverters
3. Neutral Point Clamped Multilevel Inverters
4. Other Multilevel Inverters
5. PWM Current Source Inverters
6. PWM Current Source Rectifiers
7. Voltage Source Inverter (VSI) Fed Drives
8. Current Source Inverter (CSI) Fed Drives

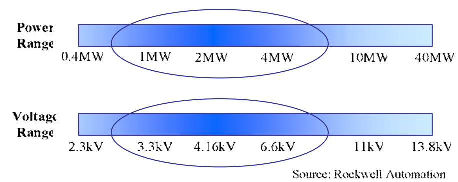
Topic 1
Introduction

Main Topics

- Medium Voltage (MV) Drive Overview
- High Power Converter Topologies
- MV Industrial Drives
- High-Power Semiconductor Devices

MV Drive Overview

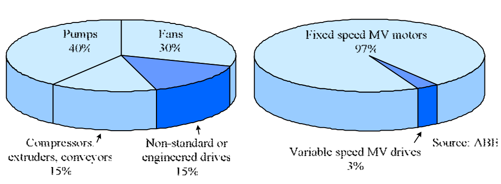
- **MV Drive Power and Voltage Ratings**



Majority of installed MV drives:
1MW to 4MW
3.3KV to 6.6KV

MV Drive Overview

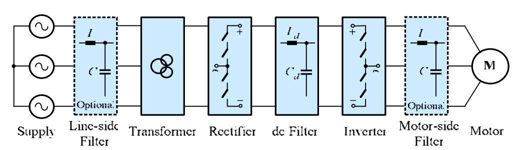
- **MV Drive Market Survey**



Main purpose for high-power fan/pump drives:
Energy conservation

MV Drive Overview

- **General Block Diagram**



Line- and motor-side filters:
Optional, depending on converter topologies and harmonic requirements

MV Drive Overview

• **MV Drive Applications**

Source: Rockwell Automation

Industry	Application Examples
Petrochemical	Pipeline pumps, gas compressors, brine pumps, mixers / extruders, electrical submersible pumps, induced draft fans, boiler feed water pumps, water injection pumps.
Cement	Kiln induced draft fans, forced draft fans, baghouse fans, preheat tower fans, raw mill induced draft fans, kiln gas fans, cooler exhaust fans, separator fans.
Mining & Metals	Slurry pumps, ventilation fans, de-scaling pumps, tandem belt conveyors, baghouse fans, cyclone feed pumps, crushers, rolling mills, hoists, coilers, winders.
Water / Wastewater	Raw sewage pumps, bio-roughing tower pumps, treatment pumps, freshwater pumps, storm water pumps.
Transportation	Propulsion for naval vessels, shuttle tankers, icebreakers, cruisers. Traction drives for locomotives, light-track trains.
Electric Power	Feed water pumps, induced draft fans, forced draft fans, effluent pumps, compressors.
Forest Products	Fan pumps, induced draft fans, boiler feed water pumps, pulpers refiners, kiln drives, line shafts.
Miscellaneous	Wind tunnels, agitators, test stands, rubber mixers.

MV Drive Overview

• **Technical Requirements and Challenges**

• **Line-Side Requirements**

Low line current THD
High input power factor

• **Motor-Side Challenges**

High *dv/dt* and wave reflection
Motor derating due to harmonics
Common-mode voltage stress

MV Drive Overview

• **Technical Requirements and Challenges**

• **Switching Device Constraints**

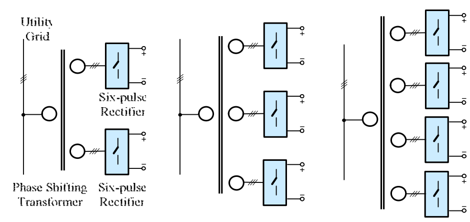
Low device Switching frequency (<1000Hz)
Reliable series connection

• **Drive System Requirements**

High efficiency
Low manufacturing cost
High reliability
Effective fault protection
Self commissioning
Minimum down-time for repairs
Small footprint
N+1 redundancy (optional)
Dynamic braking / four-quadrant operation (optional)

High-Power Converter Topologies

• **Multipulse Diode/SCR Rectifiers**



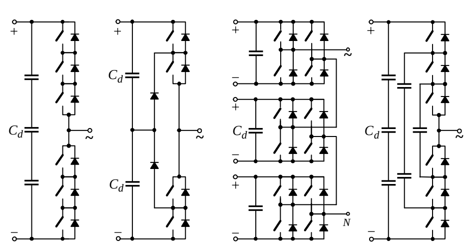
(a) 12-pulse Rectifier (b) 18-pulse Rectifier (c) 24-pulse Rectifier

Main Feature: To reduce line current THD.

Six-pulse rectifiers can be in series or isolated at their outputs, depending on inverter topologies

High-Power Converter Topologies

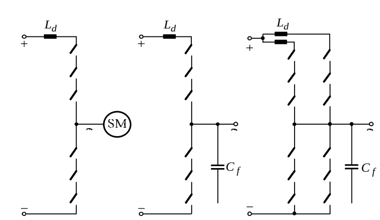
• **Multilevel Voltage Source Inverters**



Two Level Inverter | Neutral Point Clamped (NPC) Inverter | Cascaded H-bridge (CHB) Inverter | Flying Capacitor Inverter

High-Power Converter Topologies

• **PWM Current Source Inverters**



Load Commutated Inverter | PWM CSI | Dual-Bridge PWM CSI

MV Industrial Drives

• **NPC Inverter Fed MV Drive**

ACS1000, Courtesy of ABB

GCT based three-level NPC inverter fed drive (4.16KV and 1.2MW)

MV Industrial Drives

• **NPC Inverter Fed MV Drive**

SIMOVERT MV
Courtesy of Siemens

IGBT based three-level NPC inverter fed drive

MV Industrial Drives

• **CHB Inverter Fed MV Drives**

Perfect Harmony, Courtesy of ASI Robicon

IGBT based cascaded H-bridge inverter fed MV drive (4.16KV and 7.5MW)

MV Industrial Drives

• **PWM Current Source Inverter Fed Drive**

PowerFlex 7000, Courtesy of Rockwell Automation

GCT based current source based MV drive (Frame C, 2.3 MW to 7MW)

High-Power Switching Devices

• **Power Diode**

4500V/800A press-pack and 1700V/1200A module diodes

High-Power Switching Devices

• **Silicon Controlled Rectifier (SCR)**

4500V/800A and 4500V/1500A SCRs

High-Power Switching Devices

• **Gate Turn Off Thyristor (GTO)**

4500V/800A and 4500V/1500A GTOs

High-Power Switching Devices

• **Integrated Gate Controlled Thyristor (IGCT/GCT)**

6500V/1500A Symmetrical GCT

GCT = Improved GTO + Integrated Gate + Anti-parallel Diode (optional)

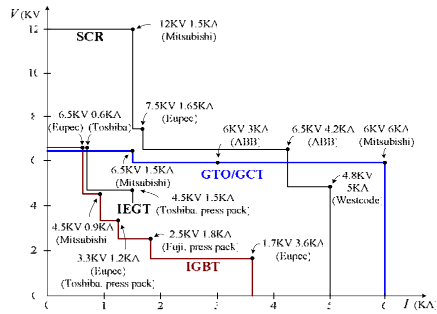
High-Power Switching Devices

• **Insulated Gate Bipolar Transistor (IGBT)**

1700V/1200A and 3300V/1200A IGBT modules

High-Power Switching Devices

• **Device Voltage/Power Ratings**



High-Power Switching Devices

• **Comparison**

Item	GTO	GCT	IGBT
Maximum voltage and current ratings	High	High	Low
Packaging	Press pack	Press pack	Module or Press pack
Switching speed	Slow	Moderate	Fast
Turn-on (*di/dt*) snubber	Required	Required	Not required
Turn-off (*dv/dt*) snubber	Required	Not required	Not required
Active overvoltage clamping	No	No	Yes
Active *di/dt* and *dv/dt* control	No	No	Yes
Active short circuit protection	No	No	Yes
On-state loss	Low	Low	High
Switching loss	High	Medium	Low
Behavior after destruction	Short circuited	Short circuited	Open circuited
Gate Driver	Complex, separate	Complex, integrated	Simple, compact
Gate Driver Power Consumption	High	Medium	Low

Topic 2
Cascaded H-Bridge (CHB) Multilevel Inverters

- **H-Bridge Inverter**
- **CHB Inverter Topologies**
- **Phase Shifted PWM**
- **Level Shifted PWM**
- **PWM Scheme Comparison**

Topic 2
CHB Multilevel Inverters

Why Use Multilevel Inverters?

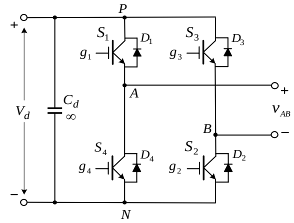
- To increase inverter operating voltage without devices in series
- To minimize THD with low switching frequencies f_{sw}
- To reduce EMI due to lower voltage steps

Device Switching frequency:

f_{sw} < 1000Hz

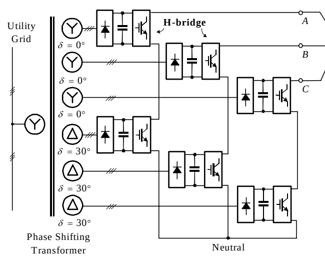
H-Bridge Inverter

- H-bridge Inverter Circuit

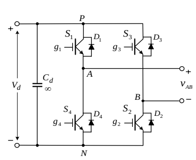


H-Bridge Inverter

- CHB Inverter Fed MV Drive



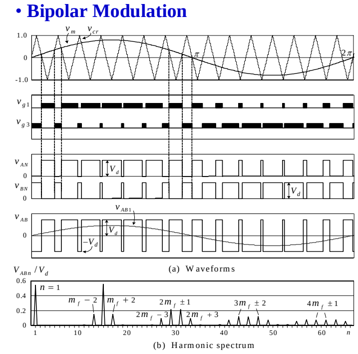
Five-level cascaded H-bridge inverter

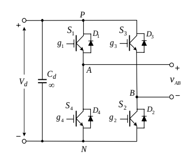


H-bridge Power Cell

H-Bridge Inverter

- Bipolar Modulation



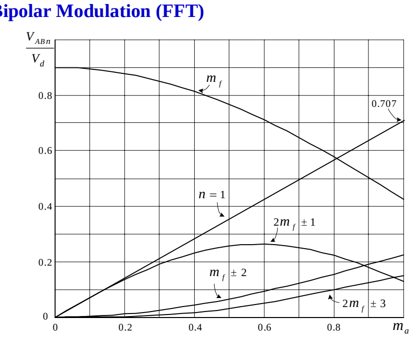


Bipolar PWM:

V_{AB} from $-V_d$ to $+V_d$ or from $+V_d$ to $-V_d$

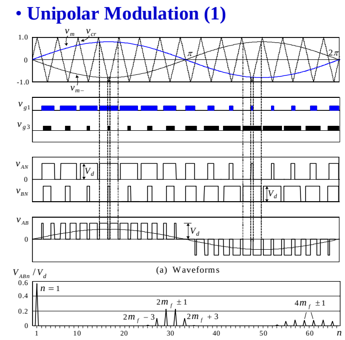
H-Bridge Inverter

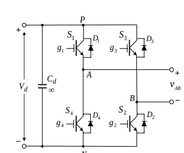
- Bipolar Modulation (FFT)



H-Bridge Inverter

- Unipolar Modulation (1)





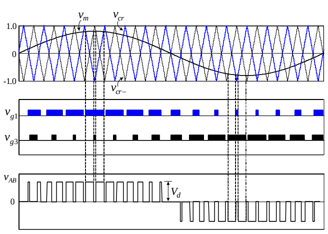
- Two modulation waves V_m and V_{m-}
- One carrier wave V_{cr}

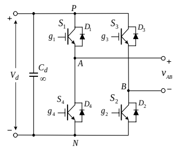
- Unipolar PWM:

V_{AB} from 0 to $+V_d$ or from 0 to $-V_d$

H-Bridge Inverter

• **Unipolar Modulation (2)**





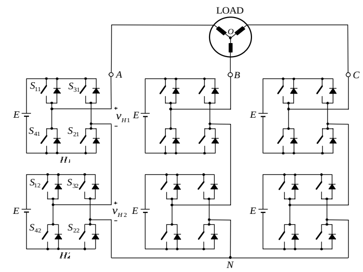
• **One modulating wave v_m**

• **Two carrier waves**

v_{cr} and v_{cr-}

CHB Inverter Topologies

• **Five-Level Inverter**



Complementary Switch pairs:
S_{11} and S_{41};
S_{31} and S_{21};

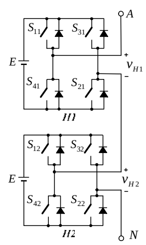
S_{12} and S_{42};
S_{32} and S_{22};

Converters in cascade, but no switching devices in series.

CHB Inverter Topologies

• **Output Voltage and Switching Status** (five-level)

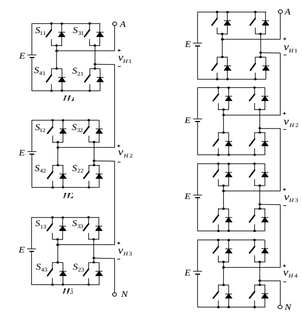
Output Voltage v_{AN}	Switching State S_{11}	S_{31}	S_{12}	S_{32}	v_{H1}	v_{H2}
2E	1	0	1	0	E	E
E	1	0	1	1	E	0
	1	0	0	0	E	0
	1	1	1	0	0	E
	0	0	1	0	0	E
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
	1	0	0	1	E	-E
	0	1	1	0	-E	E
-E	0	1	1	1	-E	0
	0	1	0	0	-E	0
	1	1	0	1	0	-E
	0	0	0	1	0	-E
-2E	0	1	0	1	-E	-E



Waveform of v_{AN} is composed of five voltage levels: *2E*, *E*, 0, *-E*, and *-2E*

CHB Inverter Topologies

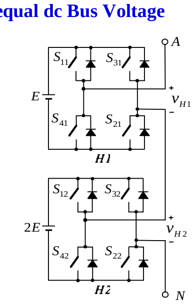
• **Seven- and Nine-Level Inverters (Per phase diagram)**



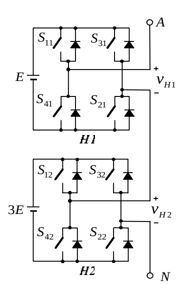
(a) Seven-level inverter (b) Nine-level inverter

CHB Inverter Topologies

• **Unequal dc Bus Voltage**



(a) Two-cell seven-level topology

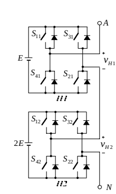


(b) Two-cell nine-level topology

CHB Inverter Topologies

• **Unequal dc Bus Voltage (Two-cell seven-level topology)**

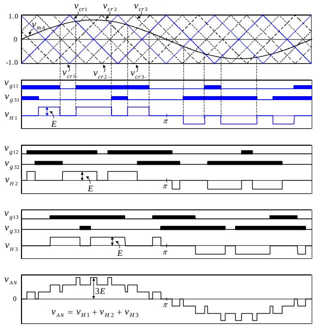
Output Voltage v_{AN}	Switching State S_{11}	S_{31}	S_{12}	S_{32}	v_{H1}	v_{H2}
3E	1	0	1	0	E	2E
2E	1	1	1	0	0	2E
	0	0	1	0	0	2E
E	1	0	1	1	E	0
	1	0	0	0	E	0
	0	1	1	0	-E	2E
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
-E	1	0	0	1	E	-2E
	0	1	1	1	-E	0
	0	1	0	0	-E	0
-2E	1	1	0	1	0	-2E
	0	0	0	1	0	-2E
-3E	0	1	0	1	-E	-2E



(a) Two-cell seven-level topology

Phase Shifted PWM

- **Multicarrier Based PWM – Phase Shifted**



- **# of voltage levels: $m = 7$**
- **# of carriers: $m_c = m - 1 = 6$**
- **Phase shift: 360°/ m_c = 60°**

Carriers for *H1* bridge: v_{cr1} and v_{cr1-}

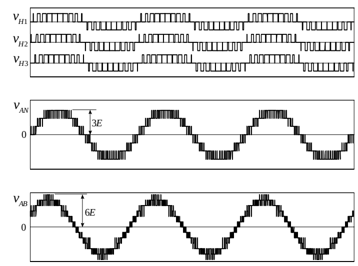
Carriers for *H2* bridge: v_{cr2} and v_{cr2-}

Carriers for *H3* bridge: v_{cr3} and v_{cr3-}

***m* = 7**

Phase Shifted PWM

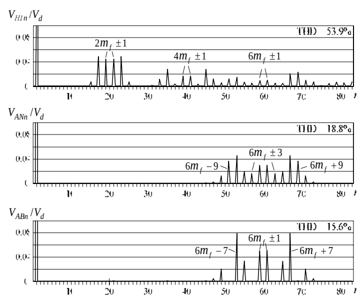
- **Waveforms** (7-level, phase shifted)



- **Switching occurs at different times**
- **$f_{sw(device)} = 60\ m_f$ = 600Hz**
- **Inverter phase voltage levels: 7**
- **Low EMI**
- **Line-to-line voltage levels: 13**
- **Close to a sinusoid**
- **Low THD**

Phase Shifted PWM

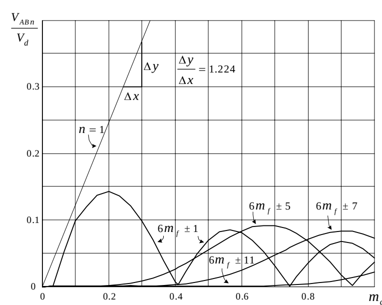
- **FFT** (7-level, phase shifted)



- **Lowest harmonics: around $2m_f$**
- **Lowest harmonics: around $6m_f$**
- **Containing triplen harmonics**
- **No triplen harmonics**
- **Equivalent $f_{sw(inverter)}$ = 60($6m_f$) = 3600Hz**

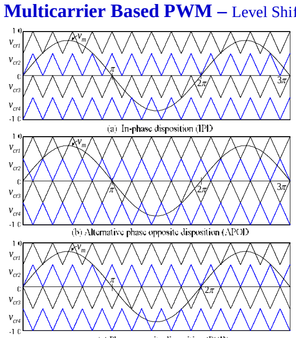
Phase Shifted PWM

- **Harmonic Content** (7-level, phase shifted)



Level Shifted PWM

- **Multicarrier Based PWM –** Level Shifted PWM



IPD

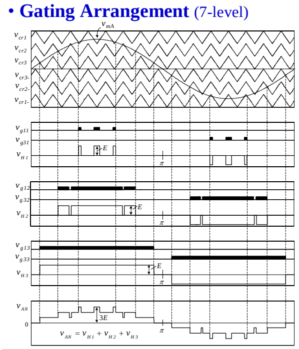
APOD

POD

- **# of voltage levels: *m = 5***
- **# of carriers: $m_c = m - 1 = 4$**
- **IPD provides the best harmonic profile.**

Level Shifted PWM

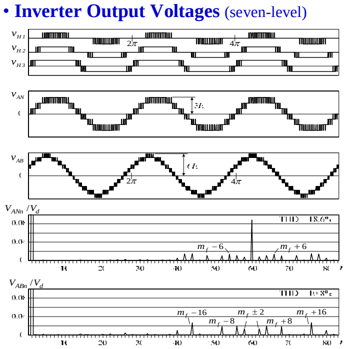
- **Gating Arrangement** (7-level)



- **# of voltage levels: *m* = 7**
- **# of carriers: $m_c = m - 1 = 6$**
- **$f_{sw(device)}$:**
  - **not equal to f_{cr}, and**
  - **not the same for all switches.**
- **Device conduction angle:**
  - **not equal.**
- **Necessary to swap switching pattern.**

Level Shifted PWM

• **Inverter Output Voltages** (seven-level)



• $m = 7$

• **Switching occurs at different times**

• $f_{sw(device)} = f_{cr} / m_c$ = **600Hz (avg)**

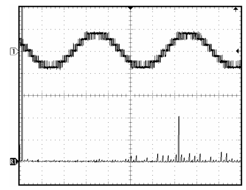
• v_{AB} **close to a sinusoid**

• **Low THD, low EMI**

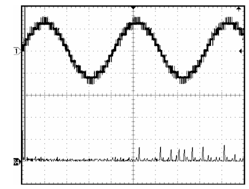
• **Equivalent** $f_{sw(inv)} = f_c$ = **3600Hz**

Level Shifted PWM

• **Measured Waveforms** (IPD, 7-level)



Inverter phase voltage v_{AZ}



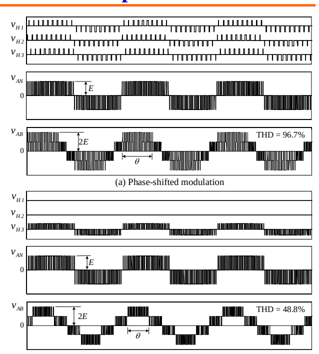
Line-to-line voltage v_{AB}

PWM Scheme Comparison

• **PWM at Low** m_a

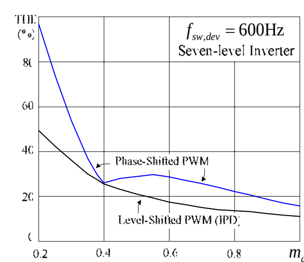
• **At** m_a **= 0.2:**

- **Phase shifted PWM: THD = 96.7%**
- **Level shifted PWM: THD = 48.8%**



PWM Scheme Comparison

• **Total Harmonic Distortion (THD)**



PWM Scheme Comparison

• **Summary**

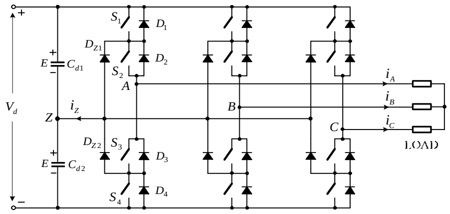
Comparison	Phase-shifted Modulation	Level-shifted Modulation (IPD)
Device Switching Frequency	Same for all devices	Different
Device Conduction Period	Same for all devices	Different
Rotating of switching patterns	No required	Required
THD of inverter output line-to-line voltage	Good	Better
Low Order Harmonics	No	Yes (Very low amplitude)

Topic 3
Neutral Point Clamped (NPC) Multilevel Inverter

• **Three-level NPC Inverter**
• **Space Vector Modulation**
• **Neutral Point Voltage Control**
• **High-level NPC Inverter**

Three-Level NPC Inverter

• **Inverter Configuration**



Clamping diodes: D_{Z1} and D_{Z2} (Phase A)

Three-Level NPC Inverter

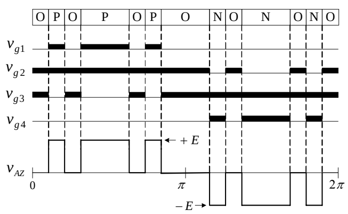
• **Switching State**

Switching State	Device Switching Status (Phase *A*)				Inverter Terminal Voltage V_{AZ}
	S_1	S_2	S_3	S_4	
P	On	On	Off	Off	E
O	Off	On	On	Off	0
N	Off	Off	On	On	$-E$

Complementary Switch pairs:
S_1 and S_3; S_2 and S_4;

Three-Level NPC Inverter

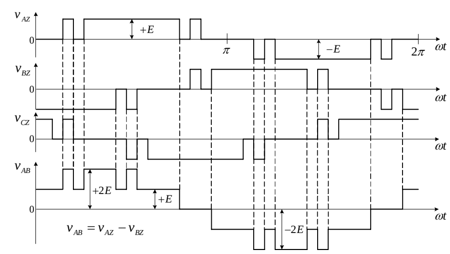
• **Gate Signal Arrangements**



Inverter phase voltage v_{AZ} has three levels: E, 0 and $-E$

Three-Level NPC Inverter

• **Inverter Output Waveforms**



Space Vector Modulation

• **Space Vectors**

• **Three-phase voltages**

$$v_{AO}(t)+v_{BO}(t)+v_{CO}(t)=0 \qquad \textbf{(1)}$$

• **Two-phase voltages**

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos 0 & \cos\frac{2\pi}{3} & \cos\frac{4\pi}{3} \\ \sin 0 & \sin\frac{2\pi}{3} & \sin\frac{4\pi}{3} \end{bmatrix}\begin{bmatrix} v_{AO}(t) \\ v_{BO}(t) \\ v_{CO}(t) \end{bmatrix} \qquad \textbf{(2)}$$

• **Space vector representation**

$$\vec{V}(t)=v_\alpha(t)+j\,v_\beta(t) \qquad \textbf{(3)}$$

(2) → (3)

$$\vec{V}(t)=\frac{2}{3}\left[v_{AO}(t)e^{j0}+v_{BO}(t)e^{j2\pi/3}+v_{CO}(t)e^{j4\pi/3}\right] \qquad \textbf{(4)}$$

where $e^{jx}=\cos x+j\sin x$

Space Vector Modulation

• **Space Vectors (Example)**

Switching state [POO] → on-state switches:
Phase A: upper two switches [P]
Phase B: lower two switches [O]
Phase C: lower two switches [O]

from which

$$v_{AO}(t)=\frac{2}{3}V_d,\; v_{BO}(t)=-\frac{1}{3}V_d \;\; \textbf{and} \;\; v_{CO}(t)=-\frac{1}{3}V_d \qquad \textbf{(5)}$$

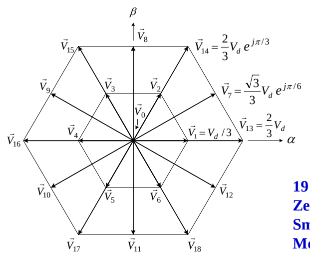
Substituting (5) to (4) gives a space vector

$$\vec{V}_1=\frac{2}{3}V_d\,e^{j0} \qquad \textbf{(6)}$$

Total switching states: 27
Total space vectors: 19

Space Vector Modulation

- **Space Vectors Diagram**



19 space vectors:
Zero vector: V_0
Small vectors: $V_1 - V_6$
Medium vectors: $V_7 - V_{12}$
Large vectors: $V_{13} - V_{18}$

Space Vector Modulation

- **Switching States and Space Vectors**

Space Vector		Switching State		Vector Classification	Vector Magnitude
$\vec{V}_0$		[PPP][OOO] [NNN]		Zero Vector (ZV)	0
		P-type	N-type	Small Vector (SV) P-type Small Vector (PSV) N-type Small Vector (NSV)	$\frac{1}{3} V_d$
$\vec{V}_1$	$\vec{V}_{1P}$	[POO]			
	$\vec{V}_{1N}$		[ONN]		
$\vec{V}_2$	$\vec{V}_{2P}$	[PPO]			
	$\vec{V}_{2N}$		[OON]		
$\vec{V}_3$	$\vec{V}_{3P}$	[OPO]			
	$\vec{V}_{3N}$		[NON]		
$\vec{V}_4$	$\vec{V}_{4P}$	[OPP]			
	$\vec{V}_{4N}$		[NOO]		
$\vec{V}_5$	$\vec{V}_{5P}$	[OOP]			
	$\vec{V}_{5N}$		[NNO]		
$\vec{V}_6$	$\vec{V}_{6P}$	[POP]			
	$\vec{V}_{6N}$		[ONO]		

Redundancy: **Zero vector – three switching states**
Small vectors – two states per vector

Space Vector Modulation

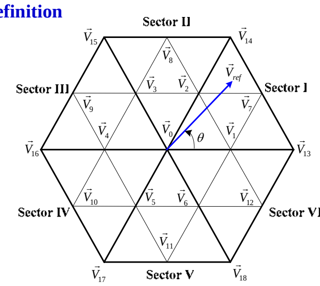
- **Switching States and Space Vectors**

Space Vector	Switching State	Vector Classification	Vector Magnitude
$\vec{V}_7$	[PON]	Medium Vector (MV)	$\frac{\sqrt{3}}{3} V_d$
$\vec{V}_8$	[OPN]		
$\vec{V}_9$	[NPO]		
$\vec{V}_{10}$	[NOP]		
$\vec{V}_{11}$	[ONP]		
$\vec{V}_{12}$	[PNO]		
$\vec{V}_{13}$	[PNN]	Large Vector (LV)	$\frac{2}{3} V_d$
$\vec{V}_{14}$	[PPN]		
$\vec{V}_{15}$	[NPN]		
$\vec{V}_{16}$	[NPP]		
$\vec{V}_{17}$	[NNP]		
$\vec{V}_{18}$	[PNP]		

No redundant switching states for medium or large vectors

Space Vector Modulation

- **Sector Definition**



V_{ref} **: Reference vector, rotating in space at a certain speed**
All other vectors are stationary

Space Vector Modulation

- **SVM Principle**

- **For a given length and position, V_{ref} can be synthesized by three nearby stationary vectors;**
- **Based on the selected stationary vectors, switching states can be designed and gate signals can be generated;**
- **When V_{ref} passes through sectors one by one, different sets of switches can be turned on or off;**
- **When V_{ref} rotates one revolution in space, the inverter output voltage varies one cycle over time;**
- **The inverter output frequency corresponds to the rotating speed of V_{ref};**
- **The inverter output voltage can be adjusted by the magnitude of V_{ref}.**

Space Vector Modulation

- **Dwell Time Calculation**

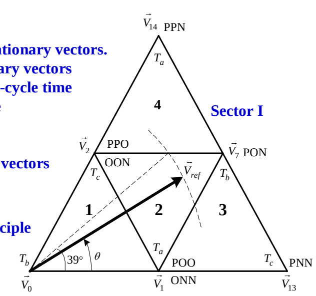
What is the dwell time?
- **V_{ref} is synthesized by three stationary vectors.**
- **The dwell time for the stationary vectors essentially represents the duty-cycle time of selected switches during the sampling period T_s.**

- **Select three nearest stationary vectors**

$\vec{V}_1, \vec{V}_2$ and $\vec{V}_7$

- **Use volt-second balancing principle**

$$\begin{cases} \vec{V}_1 T_a + \vec{V}_7 T_b + \vec{V}_2 T_c = \vec{V}_{ref} T_s \\ T_a + T_b + T_c = T_s \end{cases} \quad \text{(a)}$$



Four Regions

Space Vector Modulation

• **Dwell Time Calculation**

From equation (a)

$$\begin{cases} T_a = T_s[1-2m_a\sin\theta] \\ T_b = T_s[2m_a\sin(\frac{\pi}{3}+\theta)-1] \\ T_c = T_s[1-2m_a\sin(\frac{\pi}{3}-\theta)] \end{cases}$$

T_a, T_b and T_c – dwell times for V_1, V_7 and V_2

$m_a = \sqrt{3}\frac{V_{ref}}{V_d}$ **– modulation index**

Space Vector Modulation

• **Switching Sequence (Seven-segment)**

General Design Requirements:

a) **The transition from one switching state to the next involves only two switches in the same inverter leg, one being turned on and the other turned off; and**

b) **The transition for V_{ref} moving from one sector (or one region) to the next requires no or minimum number of switchings.**

Note:

The switching sequence design is not unique, but the above requirements should be satisfied for switching frequency minimization.

Space Vector Modulation

• **Switching Sequence (Seven-segment)**

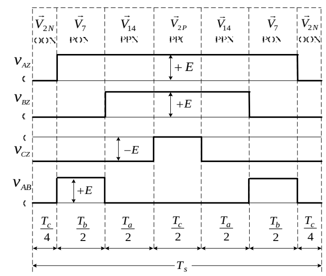
Assuming V_{ref} is in Region 4 of Sector I,

three vectors are selected: V_2, V_7 and V_{14}

Voltage Vector		$\vec{V}_{2N}$	$\vec{V}_7$	$\vec{V}_{14}$	$\vec{V}_{2P}$	$\vec{V}_{14}$	$\vec{V}_7$	$\vec{V}_{2N}$
Dwell Time		$\frac{T_c}{4}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$	$\frac{T_c}{2}$	$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{4}$
Switching State	Phase *A*	O	P	P	P	P	P	O
	Phase *B*	O	O	P	P	P	O	O
	Phase *C*	N	N	N	O	N	N	N
$[P]=E$, $[O]=0$, $[N]=-E$.								

Space Vector Modulation

• **Switching Sequence (Seven-segment)**



Switching sequence requirement *a)* is satisfied

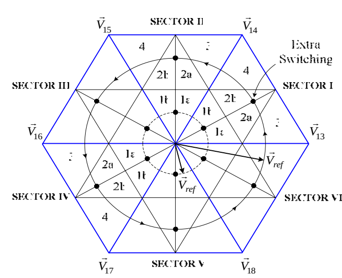
Space Vector Modulation

• **Switching Sequence (Seven-segment)**

Sector I												
Sgmt	**1a**		**1b**		**2a**		**2b**		**3**		**4**	
1st	$\vec{V}_{1N}$	[ONN]	$\vec{V}_{2N}$	[OON]	$\vec{V}_{1N}$	[ONN]	$\vec{V}_{2N}$	[OON]	$\vec{V}_{1N}$	[ONN]	$\vec{V}_{2N}$	[OON]
2nd	$\vec{V}_{2N}$	[OON]	$\vec{V}_0$	[OOO]	$\vec{V}_{2N}$	[OON]	$\vec{V}_7$	[PON]	$\vec{V}_{13}$	[PNN]	$\vec{V}_7$	[PON]
3rd	$\vec{V}_0$	[OOO]	$\vec{V}_{1P}$	[POO]	$\vec{V}_7$	[PON]	$\vec{V}_{1P}$	[POO]	$\vec{V}_7$	[PON]	$\vec{V}_{14}$	[PPN]
4th	$\vec{V}_{1P}$	[POO]	$\vec{V}_{2P}$	[PPO]	$\vec{V}_{1P}$	[POO]	$\vec{V}_{2P}$	[PPO]	$\vec{V}_{1P}$	[POO]	$\vec{V}_{2P}$	[PPO]
5th	$\vec{V}_0$	[OOO]	$\vec{V}_{1P}$	[POO]	$\vec{V}_7$	[PON]	$\vec{V}_{1P}$	[POO]	$\vec{V}_7$	[PON]	$\vec{V}_{14}$	[PPN]
6th	$\vec{V}_{2N}$	[OON]	$\vec{V}_0$	[OOO]	$\vec{V}_{2N}$	[OON]	$\vec{V}_7$	[PON]	$\vec{V}_{13}$	[PNN]	$\vec{V}_7$	[PON]
7th	$\vec{V}_{1N}$	[ONN]	$\vec{V}_{2N}$	[OON]	$\vec{V}_{1N}$	[ONN]	$\vec{V}_{2N}$	[OON]	$\vec{V}_{1N}$	[ONN]	$\vec{V}_{2N}$	[OON]
Sector II												
Sgmt	**1a**		**1b**		**2a**		**2b**		**3**		**4**	
1st	$\vec{V}_{2N}$	[OON]	$\vec{V}_{3N}$	[NON]	$\vec{V}_{2N}$	[OON]	$\vec{V}_{3N}$	[NON]	$\vec{V}_{2N}$	[OON]	$\vec{V}_{3N}$	[NON]
2nd	$\vec{V}_0$	[OOO]	$\vec{V}_{2N}$	[OON]	$\vec{V}_8$	[OPN]	$\vec{V}_{2N}$	[OON]	$\vec{V}_8$	[OPN]	$\vec{V}_{15}$	[NPN]
3rd	$\vec{V}_{3P}$	[OPO]	$\vec{V}_0$	[OOO]	$\vec{V}_{3P}$	[OPO]	$\vec{V}_8$	[OPN]	$\vec{V}_{14}$	[PPN]	$\vec{V}_8$	[OPN]
4th	$\vec{V}_{2P}$	[PPO]	$\vec{V}_{3P}$	[OPO]	$\vec{V}_{2P}$	[PPO]	$\vec{V}_{3P}$	[OPO]	$\vec{V}_{2P}$	[PPO]	$\vec{V}_{3P}$	[OPO]
5th	$\vec{V}_{3P}$	[OPO]	$\vec{V}_0$	[OOO]	$\vec{V}_{3P}$	[OPO]	$\vec{V}_8$	[OPN]	$\vec{V}_{14}$	[PPN]	$\vec{V}_8$	[OPN]
6th	$\vec{V}_0$	[OOO]	$\vec{V}_{2N}$	[OON]	$\vec{V}_8$	[OPN]	$\vec{V}_{2N}$	[OON]	$\vec{V}_8$	[OPN]	$\vec{V}_{15}$	[NPN]
7th	$\vec{V}_{2N}$	[OON]	$\vec{V}_{3N}$	[NON]	$\vec{V}_{2N}$	[OON]	$\vec{V}_{3N}$	[NON]	$\vec{V}_{2N}$	[OON]	$\vec{V}_{3N}$	[NON]

Space Vector Modulation

• **Switching Sequence (Seven-segment)**



Device switching frequency:

$f_{sw,dev} = f_{sp}/2 + f_1/2$

Sampling frequency:

$f_{sp} = 1/T_s$

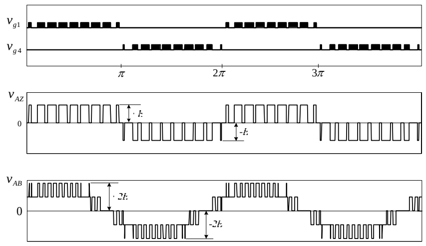
Fundamental frequency:

f_1

Switching sequence requirement *b)* is satisfied

Space Vector Modulation

- **Simulated Waveforms** (Seven-segment)

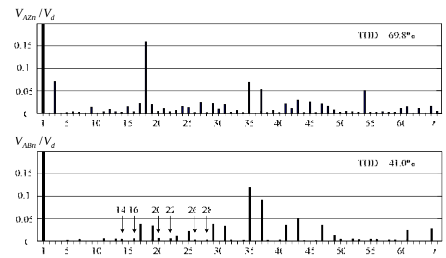


f_1 = 60Hz, T_s = 1/1080 sec, m_a = 0.8, f_{sw} = 570Hz

v_{AB} is not half wave symmetrical; and Contains both even- and odd-order harmonics

Space Vector Modulation

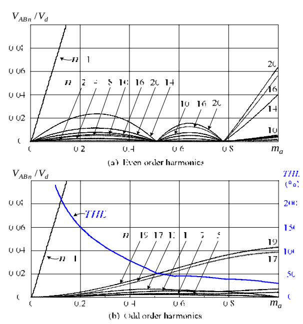
- **Simulated Waveforms** (Seven-segment)



f_1 = 60Hz, T_s = 1/1080 sec, m_a = 0.8, f_{sw} = 570Hz

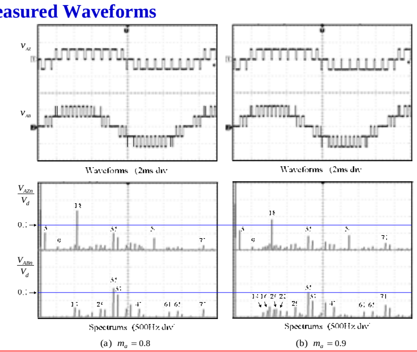
Space Vector Modulation

- **Harmonic Content** (Seven-segment)



Space Vector Modulation

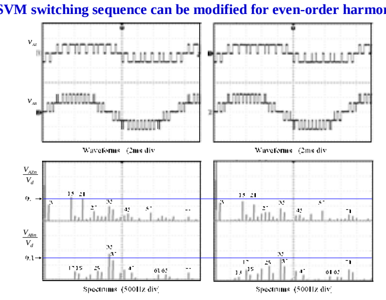
- **Measured Waveforms**



Space Vector Modulation

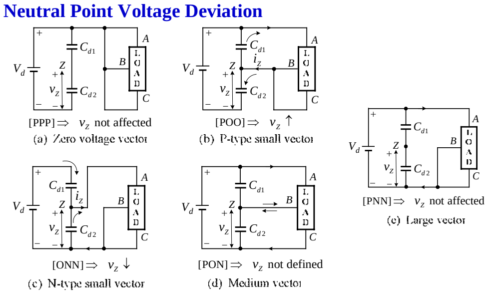
- **Measured waveforms** (No even-order harmonics)

The SVM switching sequence can be modified for even-order harmonic elimination.



Neutral Point Voltage Control

- **Neutral Point Voltage Deviation**



The neutral point voltage v_z can be controlled by P- and N-types of small vectors

Neutral Point Voltage Control

• **Neutral Point Voltage Control**

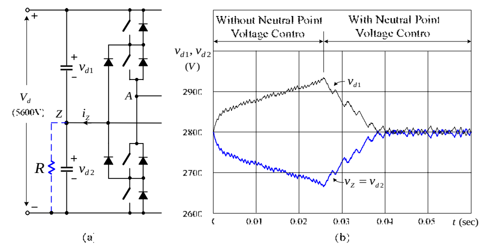
$$T_a = T_{aP} + T_{aN}$$

$$\begin{cases} T_{aP} = \dfrac{T_a}{2}(1+\Delta t) \\ T_{aN} = \dfrac{T_a}{2}(1-\Delta t) \end{cases} \qquad -1 \le \Delta T \le 1$$

Neutral Point Deviation Level	Motoring Mode $i_d > 0$	Regenerating Mode $i_d < 0$
$(v_{d1} - v_{d2}) > \Delta V_d$	$\Delta t > 0$	$\Delta t < 0$
$(v_{d2} - v_{d1}) > \Delta V_d$	$\Delta t < 0$	$\Delta t > 0$
$\lvert v_{d1} - v_{d2} \rvert < \Delta V_d$	$\Delta t = 0$	$\Delta t = 0$
ΔV – maximum allowed voltage deviation ($\Delta V_d > 0$).		

Neutral Point Voltage Control

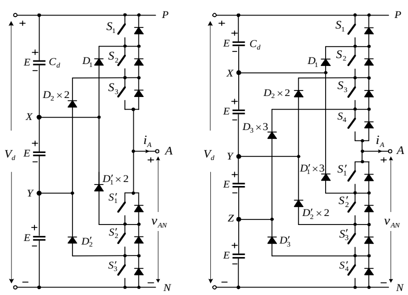
• **Neutral Point Voltage Control**



***R* is used on purpose to make the dc voltage unbalance.**

High-Level NPC Inverters

• **Inverter Topologies**



(a) Four-level (m = 4)   (b) Five-level (m = 5)

High-Level NPC Inverters

• **Switching State**

Switch Status – Four-level Inverter: S_1	S_2	S_3	S_1'	S_2'	S_3'	v_{AN}
1	1	1	0	0	0	**3E**
0	1	1	1	0	0	**2E**
0	0	1	1	1	0	***E***
0	0	0	1	1	1	**0**

Five-level Inverter: S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	v_{AN}
1	1	1	1	0	0	0	0	**4E**
0	1	1	1	1	0	0	0	**3E**
0	0	1	1	1	1	0	0	**2E**
0	0	0	1	1	1	1	0	***E***
0	0	0	0	1	1	1	1	**0**

High-Level NPC Inverters

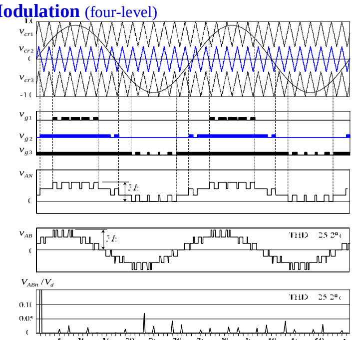
• **Component Count**

Voltage Level	Switches	Clamping Diodes*	dc capacitors
m	6(*m*-1)	3(*m*-1)(*m*-2)	(*m*-1)
3	12	6	2
4	18	18	3
5	24	36	4
6	30	60	5
* The clamping diodes have the same voltage rating as other switches.			

Note:
The number of clamping diodes increases substantially with the voltage level.

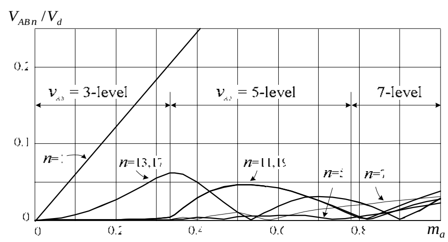
High-Level NPC Inverters

• **IPD Modulation** (four-level)



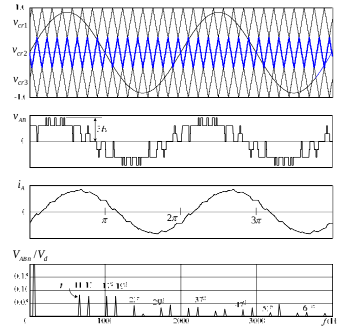
High-Level NPC Inverters

• **Harmonic Content** (four-level, IPD Modulation)



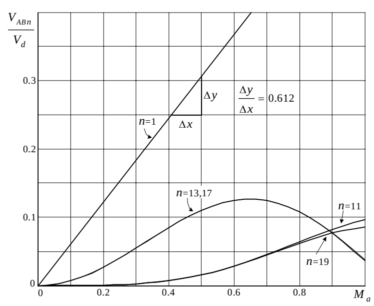
High-Level NPC Inverters

• **APOD Modulation** (four-level)



High-Level NPC Inverters

• **Harmonic Content** (four-level, APOD Modulation)



Summary

- **The three-level NPC inverter has found wide application in the MV drives.**
  Main features:
  - Low device count
  - Good harmonic profile
  - Suitable for medium voltage operation

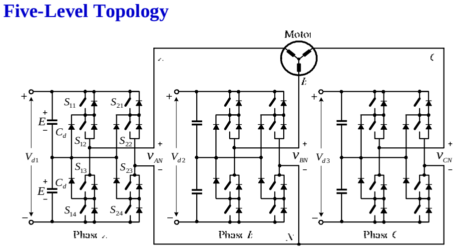
- **The practical use of four- or five-level inverters has not been reported.**
  Main reasons:
  - Difficulties in dc capacitor voltage control
  - Large number of clamping diodes

Topic 4
Other Multilevel Inverters

- **NPC/H-Bridge Inverters**
- **Flying-Capacitor Multilevel Inverters**

NPC/H-bridge Inverters

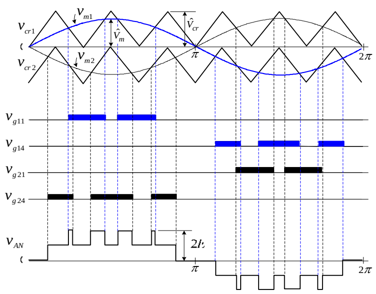
• **Five-Level Topology**



Compared with three-level NPC Topology:
- Voltage levels increases from three to five
- Inverter output voltage and power are doubled
- Device count is doubled

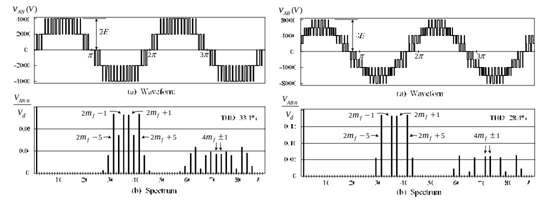
NPC/H-bridge Inverters

• IPD Modulation



NPC/H-bridge Inverters

• Waveforms and FFT

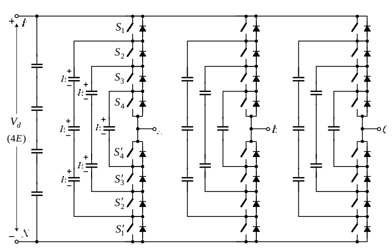


Inverter phase voltage v_{AN} : 5-levels

Line-to-line voltage v_{AN} : 9-levels

Flying Capacitor Multilevel Inverters

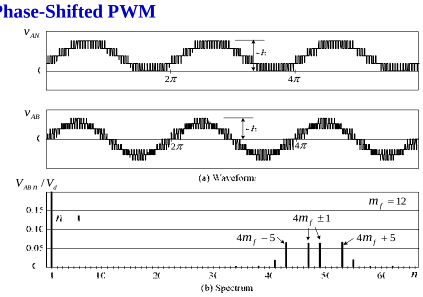
• Five-Level Topology



Complementary Switch pairs:
S_1 and S'_1;
S_2 and S'_2;
S_3 and S'_3;
S_4 and S'_4;

Flying Capacitor Multilevel Inverters

• Phase-Shifted PWM



• $f_{sw\,(device)} = 60(m_f) = 720$Hz
• $f_{sw\,(inverter)} = 60(4m_f) = 2880$Hz

Flying Capacitor Multilevel Inverters

• Summary

Features:
- Low harmonic distortion
- Modular design

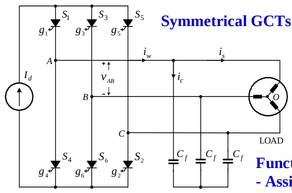
Drawbacks:
- Large number of dc caps
- Complex pre-charging circuits
- Difficulties in dc cap voltage balancing control

Topic 5
PWM Current Source Inverters (CSI)

Main Topics
- Single Bridge Inverter
- Trapezoidal Modulation (TPWM)
- Selective Harmonic Elimination (SHE)
- Space Vector Modulation (SVM)
- Dual Bridge Inverter

Single Bridge Inverter

• **Inverter Topology**



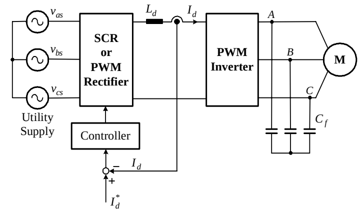
Symmetrical GCTs

Function of C_f:
- Assist GCT commutation
- Reduce harmonic distortion

Features:
- Simple topology – no antiparallel diodes
- Reliable short circuit protection – constant dc current
- Very low *dv/dt* on motor terminals

Single Bridge Inverter

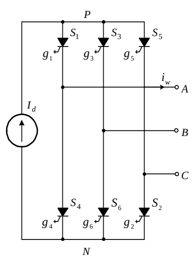
• **DC Current Source I_d**



Implementation of dc current source:
- use a large size dc choke – making I_d smooth;
- use dc current feed back control – keeping I_d constant

Single Bridge Inverter

• **Modulation Techniques**



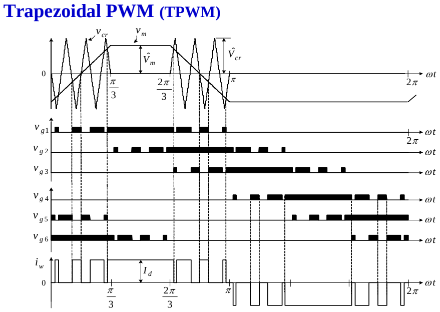
• **Trapezoidal PWM (TPWM)**
• **Selective Harmonic Elimination (SHE)**
• **Space Vector Modulation (SVM)**

• **Constraints on Switching Pattern Design**
- dc current I_d cannot be interrupted
- inverter output current waveform must be defined.

• **At any time instant, only two switches are turned on, one connected to the positive dc bus, and the other to the negative dc bus.**

Trapezoidal Modulation

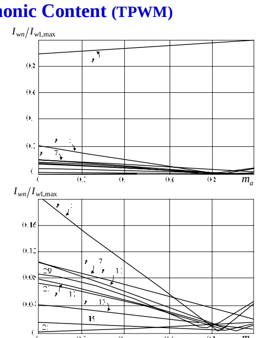
• **Trapezoidal PWM (TPWM)**



Number of pulses per half cycle: $N_p = 7$

Trapezoidal Modulation

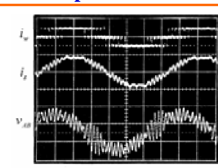
• **Harmonic Content (TPWM)**



• **$N_p = 15$**
• **Fundamental does not change much with m_a**
• **$m_a = 0.85$**

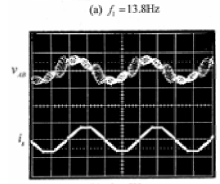
Trapezoidal Modulation

• **Waveforms**
(TPWM)



(a) $f_1 = 13.8$Hz

$f_1 = 13.8\text{Hz}, N_p = 13,$
$f_{sw} = 180\text{Hz}$

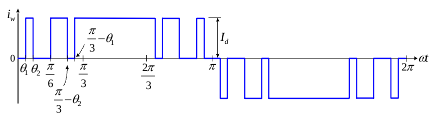


(b) $f_1 = 5$Hz

$f_1 = 5\text{Hz}, N_p = 31,$
$f_{sw} = 155\text{Hz}$

Selective Harmonic Elimination

- **Selective Harmonic Elimination** (SHE)



- **Not all the switching angles are independent.**
- **Only two harmonics can be eliminated with $N_p = 5$.**
- **Number of harmonics to be eliminated:** $k = (N_p - 1)/2$
- **No modulation index control – the magnitude of inverter output current is controlled by I_d**

Selective Harmonic Elimination

- **Fourier Analysis**

$$i_w(\omega t) = \sum_{n=1}^{\infty} a_n \sin(n\omega t)$$

$$a_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} i_w(\omega t)\sin(n\omega t)d(\omega t)$$

$$a_n = \frac{4I_{dc}}{\pi}\times\begin{cases}\int_{\theta_1}^{\theta_2}\sin(n\omega t)d(\omega t)+...+\int_{\theta_k}^{\frac{\pi}{6}}\sin(n\omega t)d(\omega t)+ \\ \int_{\frac{\pi}{3}-\theta_k}^{\frac{\pi}{3}-\theta_{k-1}}\sin(n\omega t)d(\omega t)+...+\int_{\frac{\pi}{3}-\theta_1}^{\frac{\pi}{2}}\sin(n\omega t)d(\omega t) & \text{k = odd;} \\ \int_{\theta_1}^{\theta_2}\sin(n\omega t)d(\omega t)+...+\int_{\theta_{k-1}}^{\theta_k}\sin(n\omega t)d(\omega t)+ \\ \int_{\frac{\pi}{6}}^{\frac{\pi}{3}-\theta_k}\sin(n\omega t)d(\omega t)+...+\int_{\frac{\pi}{3}-\theta_1}^{\frac{\pi}{2}}\sin(n\omega t)d(\omega t) & \text{k = even.}\end{cases}$$

Selective Harmonic Elimination

- **Fourier Analysis**

Expression for a_n

$$a_n = \frac{4I_{dc}}{\pi n}\times\begin{cases}\cos(n\theta_1)+\cos[n(\frac{\pi}{3}-\theta_1)]-\cos(n\theta_2)-\cos[n(\frac{\pi}{3}-\theta_2)]+... \\ +\cos(n\theta_k)+\cos[n(\frac{\pi}{3}-\theta_k)]-\cos(n\frac{\pi}{6}) & \text{k = odd;} \\ \cos(n\theta_1)+\cos[n(\frac{\pi}{3}-\theta_1)]-\cos(n\theta_2)-\cos[n(\frac{\pi}{3}-\theta_2)]+... \\ -\cos(n\theta_k)-\cos[n(\frac{\pi}{3}-\theta_k)]+\cos(n\frac{\pi}{6}) & \text{k = even.}\end{cases}$$

Selective Harmonic Elimination

- **Switching Angle Calculation**

To Eliminate n^{th} harmonic, set $a_n = 0$

$$F_i(\theta_1, \theta_2, \theta_3, ..., \theta_k) = 0 \qquad i = 1, 2, ..., k$$

For 5th, 7th and 11th harmonic elimination:

$$F_1 = \cos(5\theta_1)+\cos[5(\frac{\pi}{3}-\theta_1)]-\cos(5\theta_2)-\cos[5(\frac{\pi}{3}-\theta_2)]+$$
$$+\cos(5\theta_3)+\cos[5(\frac{\pi}{3}-\theta_3)]-\cos(\frac{5\pi}{6})=0$$

$$F_2 = \cos(7\theta_1)+\cos[7(\frac{\pi}{3}-\theta_1)]-\cos(7\theta_2)-\cos[7(\frac{\pi}{3}-\theta_2)]$$
$$+\cos(7\theta_3)+\cos[7(\frac{\pi}{3}-\theta_3)]-\cos(\frac{7\pi}{6})=0$$

$$F_3 = \cos(11\theta_1)+\cos[11(\frac{\pi}{3}-\theta_1)]-\cos(11\theta_2)-\cos[11(\frac{\pi}{3}-\theta_2)]$$
$$+\cos(11\theta_3)+\cos[11(\frac{\pi}{3}-\theta_3)]-\cos(\frac{11\pi}{6})=0$$

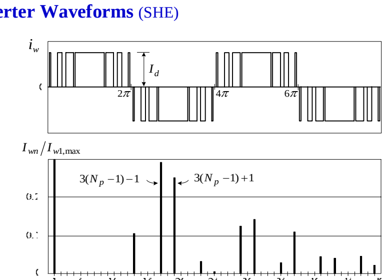
Selective Harmonic Elimination

- **Switching Angles** (SHE)

Harmonics Eliminated	Switching Angles			Harmonics Eliminated	Switching Angles			
	θ_1	θ_2	θ_3		θ_1	θ_2	θ_3	θ_4
5	18.00	-	-	7,11,17	11.70	14.12	24.17	-
7	21.43	-	-	7,13,17	12.69	14.97	24.16	-
11	24.55	-	-	7,13,19	13.49	15.94	24.53	-
13	25.38	-	-	11,13,17	14.55	15.97	25.06	-
5,7	7.93	13.75	-	11,13,19	15.24	16.71	25.32	-
5,11	12.96	19.14	-	13,17,19	17.08	18.23	25.84	-
5,13	14.48	21.12	-	13,17,23	18.03	19.22	26.16	-
7,11	15.23	19.37	-	5,7,11,13	0.00	1.60	15.14	20.26
7,13	16.58	20.79	-	5,7,11,17	0.07	2.63	16.57	21.80
7,17	18.49	23.08	-	5,7,11,19	1.11	4.01	18.26	23.60
11,13	19.00	21.74	-	5,7,13,17	1.50	4.14	16.40	21.12
11,17	20.51	23.14	-	5,7,13,19	2.56	5.57	17.82	22.33
11,19	21.10	23.75	-	5,7,17,19	4.59	7.96	17.17	20.55
13,17	21.19	23.45	-	5,11,13,17	4.16	6.07	16.79	22.04
13,19	21.71	23.94	-	5,11,13,19	5.13	7.26	17.57	22.72
5,7,11	2.24	5.60	21.26	5,11,17,19	6.93	9.15	17.85	22.77
5,7,13	4.21	8.04	22.45	5,13,17,19	7.80	9.82	18.01	23.25
5,7,17	6.91	11.96	25.57	7,11,13,17	5.42	6.65	18.03	22.17
5,11,13	7.81	11.03	22.13	7,11,13,19	6.35	7.69	18.67	22.74
5,11,17	10.16	14.02	23.34	7,11,17,19	8.07	9.44	19.09	22.93
5,13,17	11.24	14.92	22.98	7,13,17,19	8.88	10.12	19.35	23.22
7,11,13	9.51	11.64	23.27	11,13,17,19	10.39	11.14	20.56	23.60

Selective Harmonic Elimination

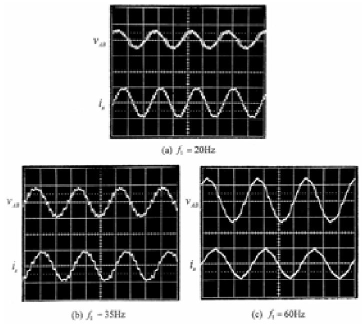
- **Inverter Waveforms** (SHE)



Harmonic eliminated: 5th, 7th and 11th; f_{sw} = 420Hz

Selective Harmonic Elimination

• **Waveforms** (SHE)



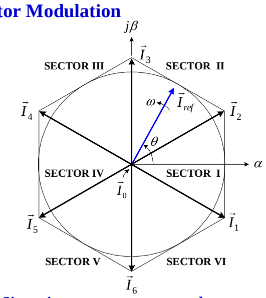
(a) $f_1 = 20Hz,\ N_p = 7$
$I_{w5} = I_{w7} = I_{w11} = 0$

(b) $f_1 = 35Hz,\ N_p = 5$
$I_{w5} = I_{w7} = 0$

(c) $f_1 = 60Hz,\ N_p = 3$
$I_{w5} = 0$

Space Vector Modulation

• **Space Vector Modulation**

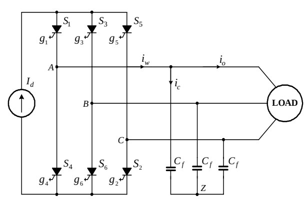


• **Six active current vectors and one zero vector**
• **Six sectors.**

Space Vector Modulation

• **Switching State**

Switching State	Leg A		
	S_1	S_4	I_w
[1]	On	Off	I_d
[-1]	Off	On	$-I_d$
[0]	Off	Off	0
[2]	On	On	0



Space Vector Modulation

• **Switching States and Space Vectors**

Space Vector		Switching State	On-state Switch	Vector Definition
Zero Vector	$\vec{I}_0$	[2 0 0]	S_1, S_4	$\vec{I}_0 = 0$
		[0 2 0]	S_3, S_6	
		[0 0 2]	S_5, S_2	
Active Vector	$\vec{I}_1$	[1 -1 0]	S_6, S_1	$\vec{I}_1 = \frac{2}{\sqrt{3}} I_d\, e^{-j\pi/6}$
	$\vec{I}_2$	[1 0 -1]	S_1, S_2	$\vec{I}_2 = \frac{2}{\sqrt{3}} I_d\, e^{j\pi/6}$
	$\vec{I}_3$	[0 1 -1]	S_2, S_3	$\vec{I}_2 = \frac{2}{\sqrt{3}} I_d\, e^{j3\pi/6}$
	$\vec{I}_4$	[-1 1 0]	S_3, S_4	$\vec{I}_4 = \frac{2}{\sqrt{3}} I_d\, e^{j5\pi/6}$
	$\vec{I}_5$	[-1 0 1]	S_4, S_5	$\vec{I}_5 = \frac{2}{\sqrt{3}} I_d\, e^{j7\pi/6}$
	$\vec{I}_6$	[0 -1 1]	S_5, S_6	$\vec{I}_6 = \frac{2}{\sqrt{3}} I_d\, e^{j9\pi/6}$

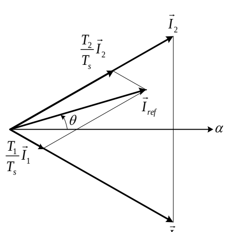
[1]: Upper switch on
[-1]: Lower switch on
[0]: None of the switches in a leg turned on
[2]: Both switches in a leg turned on (bypass mode)

Space Vector Modulation

• **Dwell Time Calculation**

Following the same principle of SVM for the NPC inverter

$$\begin{cases} \vec{I}_{ref}\, T_s = \vec{I}_1 T_1 + \vec{I}_2 T_2 + \vec{I}_0 T_0 \\ T_s = T_1 + T_2 + T_0 \end{cases}$$



$$\begin{cases} \textbf{Re:} & I_{ref}(\cos\theta) T_s = I_d (T_1 + T_2) \\ \textbf{Im:} & I_{ref}(\sin\theta) T_s = \frac{1}{\sqrt{3}} I_d (-T_1 + T_2) \end{cases}$$

Space Vector Modulation

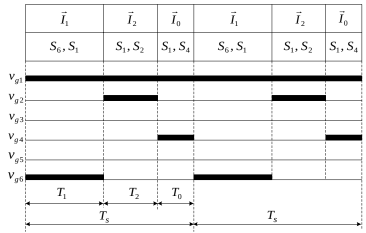
• **Dwell Time Calculation**

$$\begin{cases} T_1 = \frac{I_{ref}}{I_d} \sin(\frac{\pi}{6} - \theta) T_s \\ T_2 = \frac{I_{ref}}{I_d} \sin(\frac{\pi}{6} + \theta) T_s \\ T_0 = T_s - T_1 - T_2 \end{cases} \rightarrow \begin{cases} T_1 = m_a \sin(\frac{\pi}{6} - \theta) T_s \\ T_2 = m_a \sin(\frac{\pi}{6} + \theta) T_s \\ T_0 = T_s - T_1 - T_2 \end{cases}$$

$$m_a = \frac{I_{ref}}{I_d} = \frac{\hat{I}_{w1}}{I_d}$$

Space Vector Modulation

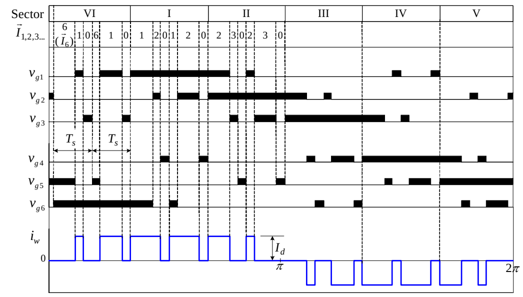
• **Switching Sequence**



Requirements:
1) **Transition from one switching state to the next involves only two switches**
2) **At any time only two switches are on.**

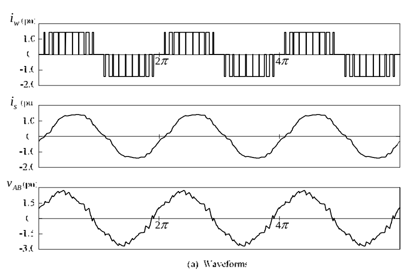
Space Vector Modulation

• **Switching Sequence (Over one cycle)**



Space Vector Modulation

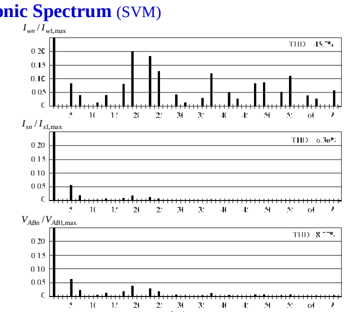
• **Inverter Output Waveforms** (SVM)



f_1 = 60Hz, f_{sw} = 540Hz, N_p = 9 and m_a = 1

Space Vector Modulation

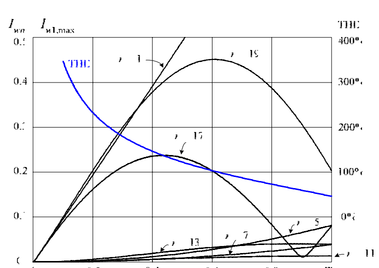
• **Harmonic Spectrum** (SVM)



f_1 = 60Hz, f_{sw} = 540Hz, N_p = 9 and m_a = 1

Space Vector Modulation

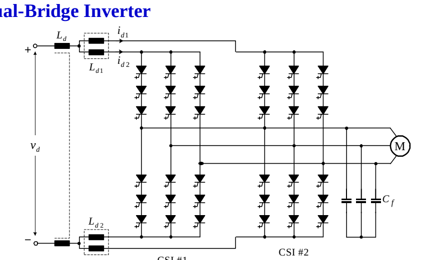
• **Harmonic Content** (SVM)



(a) f_{sw} = 540Hz, N_p = 9

Dual Bridge Inverter

• **Dual-Bridge Inverter**



Research focus
- **Increase converter power rating**
- **Equal dc current sharing**
- **Switching pattern optimization**

Summary

• **CSI PWM Schemes**

Item	SVM	TPWM	SHE
DC Current Utilization $I_{wl,max}/I_d$	0.707	0.74	0.73 to 0.78
Dynamic performance	High	Medium	Low
Digital Implementation	Real time	Real time or look-up table	Look-up table
Harmonic Performance	Adequate	Good	Best
dc Current Bypass Operation	Yes	No	Optional

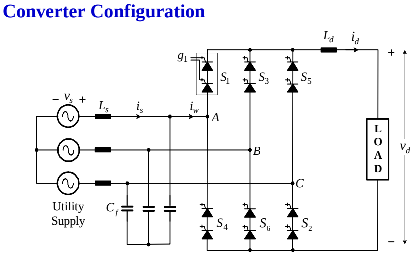
Topic 6
Current Source Rectifier

Topics

• **Single Bridge Rectifier**
• **Dual Bridge Rectifier**
• **Power Factor Control**
• **LC Resonance and Active Damping**

Single Bridge Rectifier

• **Converter Configuration**

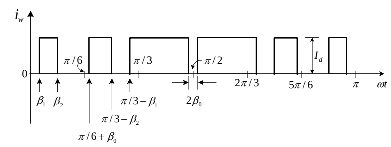


• **Switching devices: Symmetrical GCT**

• **Function C_f**
To assist GCT commutation;
To reduce line current THD.

Single Bridge Rectifier

• **Rectifier Input Current Waveform**

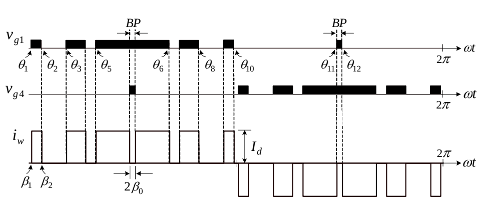


• **Constraints for Switching Pattern Design**
- **dc current i_d should not be interrupted**
- **waveform of i_w should be defined**

• **Three independent angles to eliminate two harmonics and make modulation index adjustable.**

Single Bridge Rectifier

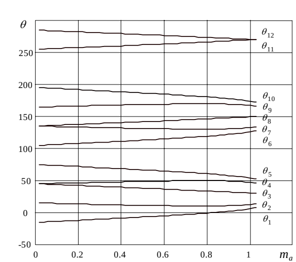
• **Switching Angles**



• **Bypass pulse (BP) - make i_w adjustable**

Single Bridge Rectifier

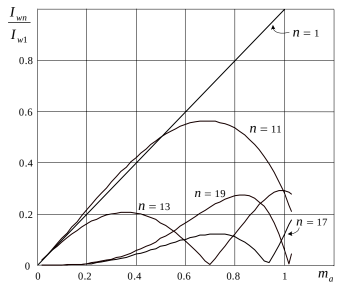
• **Switching Angles *versus* m_a**



(5[th] and 7[th] harmonic elimination)

Single Bridge Rectifier

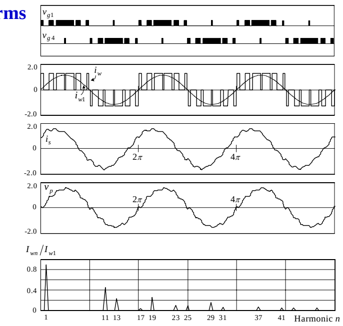
• **Harmonic Profile**



(5th and 7th harmonic elimination)

Single Bridge Rectifier

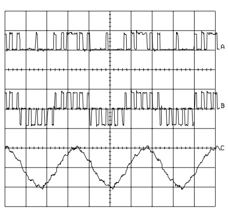
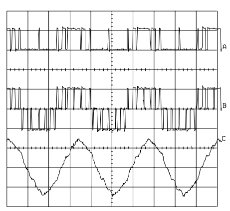
• **Waveforms**



(5th and 7th harmonic elimination)

Single Bridge Rectifier

• **Experiments**

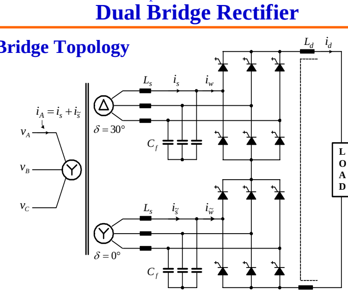



m_a = 0.7 **m_a = 0.95**

Trace A: current in switch S_1
Trace B: Rectifier input current i_w
Trace C: Line current i_s

Dual Bridge Rectifier

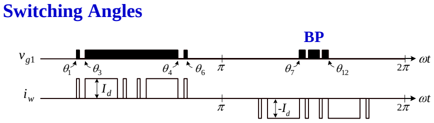
• **Dual-Bridge Topology**



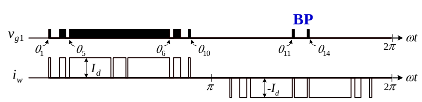
- **Use 12-pulse transformer to cancel the 5th and 7th harmonics**
- **Use PWM to eliminate the 11th and 13th harmonics**
- **The lowest harmonic in the line current is the 17th**
- **Very low line current harmonic distortion**

Dual Bridge Rectifier

• **Switching Angles**



(a) Switching pattern A for a low m_a

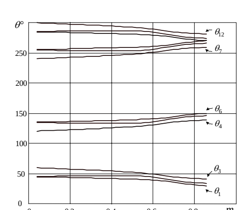
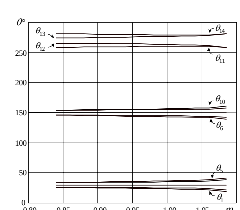


(b) Switching pattern B for a high m_a

- **Bypass pulses (BP) – make i_w adjustable**
- **SHE modulation – eliminate the 11th and 13th harmonics**

Dual Bridge Rectifier

• **Switching Angles *versus* m_d**

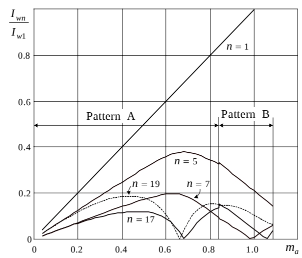



Switching pattern A **Switching pattern B**

(11th and 13th harmonic elimination)

Dual Bridge Rectifier

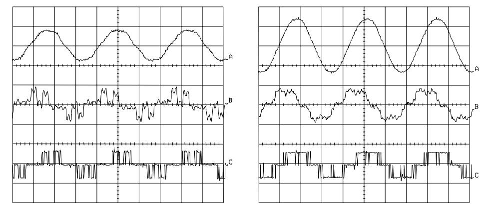
• **Harmonic Profile**



(11th and 13th harmonic elimination)

Dual Bridge Rectifier

• **Experimental Waveforms**

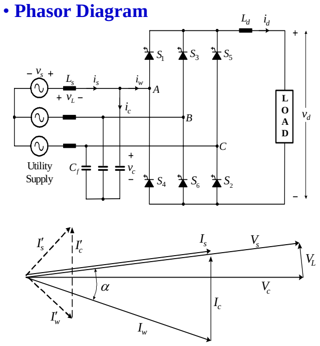


Modulation index: 0.5 **Modulation index: 0.9**

Trace A: i_A - line current on transformer primary side
Trace B: i_s - line current on transformer secondary side
Trace C: i_w - rectifier input current

Power Factor Control

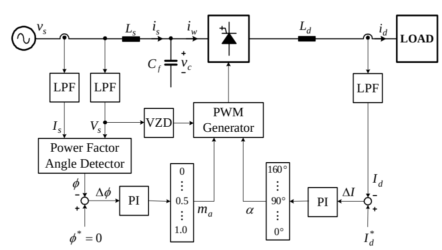
• **Phasor Diagram**



- **C_f produces leading PF**
- **Delay angle control produces lagging PF**
- **To improve PF, use m_a and delay angle control simultaneously**

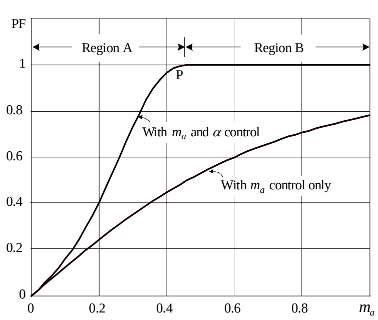
Power Factor Control

• **Block Diagram**



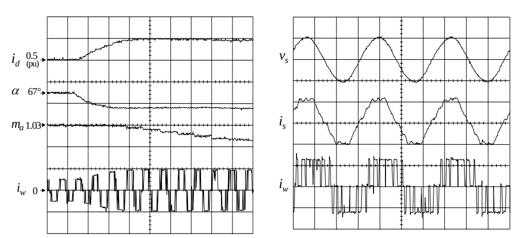
Power Factor Control

• **Power Factor Profile**



Power Factor Control

• **Experiments**

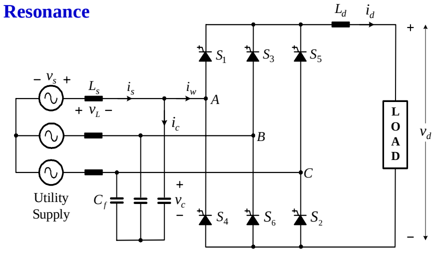


(a) Transient response

(b) Steady state waveforms (PF = 1)

LC Resonance and Active Damping

• **LC Resonance**

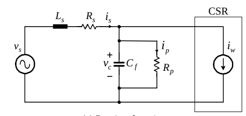


Resonant Mode: $\omega_{res} = \dfrac{1}{2\pi\sqrt{L_s C_f}}$

Resonance may be excited by
- Supply voltage harmonics
- Rectifier current harmonics

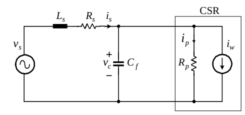
LC Resonance and Active Damping

• **Passive and Active Damping**



(a) Passive damping

• **Passive damping:**
R_p – physical damping resistor

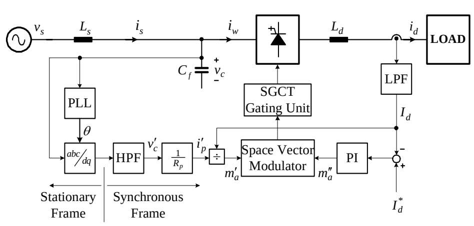


(b) Active damping

• **Active damping:**
- no physical resistor
- damping current i_p is produced by CSR via m_a control
- i_p is in phase with v_c

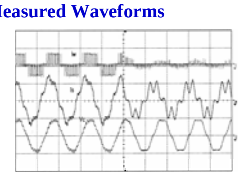
LC Resonance and Active Damping

• **Block Diagram of Active Damping Control**

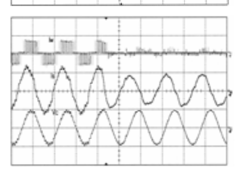


LC Resonance and Active Damping

• **Measured Waveforms**



Without Active Damping
- Rectifier input current
- Line current
- Capacitor voltage



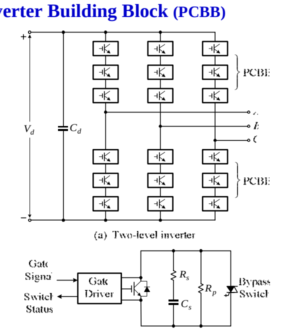
With Active Damping
- Rectifier input current
- Line current
- Capacitor voltage

Topic 7
Voltage Source Inverter Fed Drives

Topics
• **Two-Level VSI Fed Drives**
• **NPC Inverter Fed Drives**
• **CHB Inverter Fed Drives**

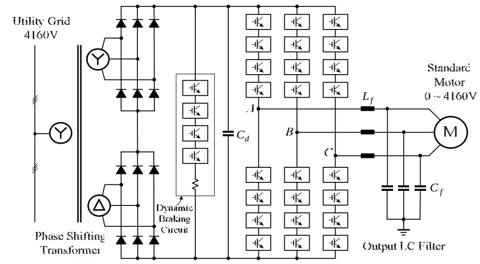
Two-Level Inverter Fed Drives

• **Power Converter Building Block (PCBB)**



Two-Level Inverter Fed Drives

• **Drive Configuration**



Two-Level Inverter Fed Drives

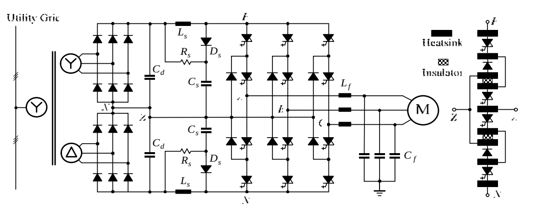
• **Features and Drawbacks**

Features
- **Modular structure using PCBB**
- **Simple PWM Scheme**
- **Active voltage clamping for series connected IGBTs**
- **N+1 Provision**
- **Ease of dc capacitor precharging**
- **Provision for four-quadrant operation and regenerative braking**

Drawbacks
- **High *dv/dt* in the inverter output voltage**
- **Large size output LC filter**

NPC Inverter Fed Drives

• **Drive Configuration (with GCT Inverter)**



(a) Drive configuration (b) Mechanical assembly

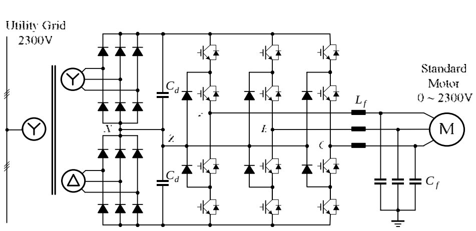
NPC Inverter Fed Drives

• **Main Specifications (With GCT Inverter)**

Nominal input voltage	2300V, 3300V, 4160V
Output power rating	400 ~ 6700HP (0.3 ~ 5 MW)
Output voltage rating	0 ~ 2300V, 0 ~ 3300V, 0 ~ 4160V
Output frequency	0 ~ 66Hz (up to 200Hz optional)
Drive system efficiency	Typically > 98.0% (including output filter losses but excluding transformer losses)
Input power factor	> 0.95% (Displacement power factor > 0.97)
Output waveform	Sinusoidal (with output filter)
Motor type	Induction or synchronous
Overload capability	Standard: 10% for one minute every 10 minutes Optional: 150% for one minute every 10 minutes
Cooling	Forced air or liquid
Mean time between failure (MTBF)	> 6 years
Regenerative braking capability	No

NPC Inverter Fed Drives

• **Drive Configuration (With IGBT Inverter)**



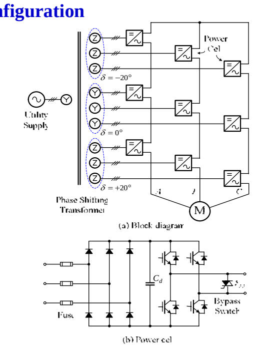
NPC Inverter Fed Drives

• **Main Specifications (With IGBT Inverter)**

Rectifier	Standard: 12-pulse diode rectifier Optional: 24-pulse diode rectifier or active front end (PWM IGBT rectifier)
Displacement power factor ($\cos\varphi$)	> 0.96 (12-pulse diode rectifier)
Nominal utility/motor voltage	2300V, 3300V, 4160V, 6600V
Output power rating	0.8 ~ 2.4MW @2300V 1.0 ~ 3.1MW @3300V 1.3 ~ 4.0MW @4160V 4.7 ~ 7.2MW @4160V (Parallel converter configuration) 0.6 ~ 2.0MW @6600V
Output voltage range	0 ~ 2300V, 0 ~ 3300V, 0 ~ 4160V, 0 ~ 6600V
Output frequency	0 ~100Hz (standard)
Motor speed range	1:1000 (with encoder)
Drive system efficiency	Typically > 98.5% (at rated operating point, excluding transformer losses)

CHB Inverter Fed Drives

• **Drive Configuration**



CHB Inverter Fed Drives

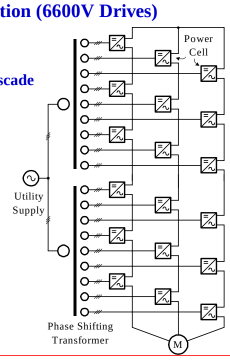
• **Drive Configuration**

	Multipulse Diode Rectifier			Multilevel CHB Inverter					
Rated Utility/Motor Voltage	Rectifier Pulses	Secondary Windings	Transformer Secondary Cables	Power Cells	IGBTs	Voltage Levels	Rated H-Bridge Output	$f_{sw,IGBT}$	$f_{sw,inv}$
2300V	18	9	27	9	36	7	480V	600Hz	3600Hz
3300V	24	12	36	12	48	9	480V	600Hz	4800Hz
4160V	30	15	45	15	60	11	480V	600Hz	6000Hz
Typical power range: 0.3 ~ 10MW (400 ~ 14000HP)									

CHB Inverter Fed Drives

• **Drive Configuration (6600V Drives)**

Two units of 3300V CHB inverter in cascade



CHB Inverter Fed Drives

• **Features and Drawbacks**

Features
- **Modular design for cost reduction**
- **Nearly sinusoidal inputs and outputs without LC filters**
- **Provision for N+1 design for high reliability**

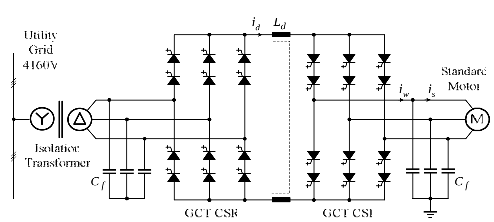
Drawbacks
- **Costly phase shifting transformers**
- **Large number of cables between transformer secondaries and power converters**
- **The transformer normally installed inside cabinet – larger footprint, more cooling requirement**

Topic 8
Current Source Inverter Fed Drives

Main Topics
- **CSI Drive for Standard Motors**
- **CSI Drive for Inverter-Duty Motors**
- **Transformerless CSI Drives for Std Motors**
- **CSI Drive with SCR Rectifiers**

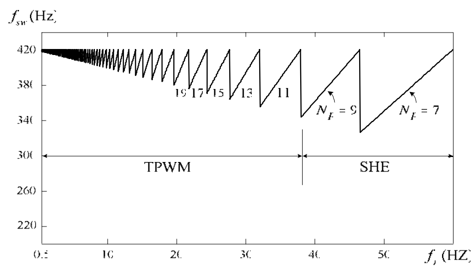
CSI Drives for Standard Motors

• **Drive Configuration**



CSI Drives for Standard Motors

• **Inverter Switching Scheme**



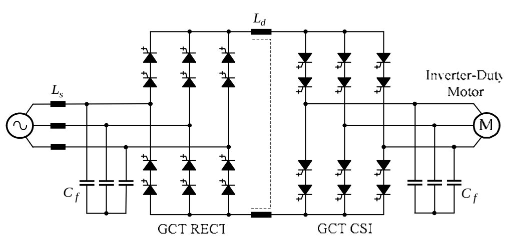
CSI Drives for Standard Motors

• **Main Specifications**

Nominal input voltage	2300V, 3300V, 4160V, 6600V
Output power rating	200 ~ 9000HP (150 ~ 6700 kW)
Output voltage rating	0 ~ 2300V, 0 ~ 3300V, 0 ~ 4160V, 0 ~ 6600V
Output frequency	0.2 ~ 85 Hz
Drive system efficiency	> 96.0% (including transformer losses)
Input power factor	Typically >0.98% (with PWM rectifier)
Line current THD	Typically <5% (with PWM rectifier)
Output waveform	Near sinusoidal current & voltage
Motor type	Induction or synchronous
Overload capability	150% - one minute (standard)
Power loss ride-through	5 cycles
Cooling	Forced air or liquid
Regenerative braking capability	Inherent. No additional hardware or software required.

CSI Drives for Inverter-Duty Motors

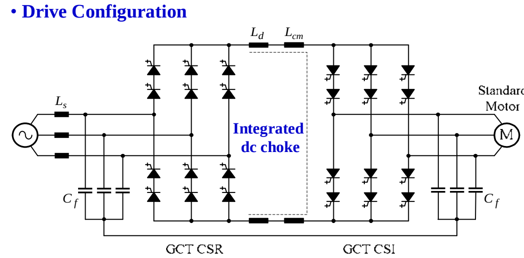
• **Drive Configuration**



No isolation transformer for cost reduction

Transformerless CSI Drives for Std Motors

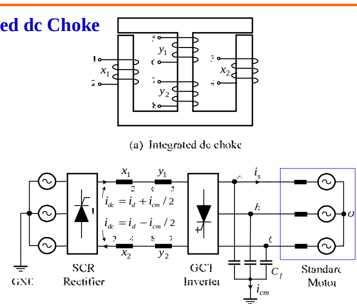
• **Drive Configuration**



Use Integrated DC choke to block common-mode voltages

Transformerless CSI Drives for Std Motors

• **Integrated dc Choke**



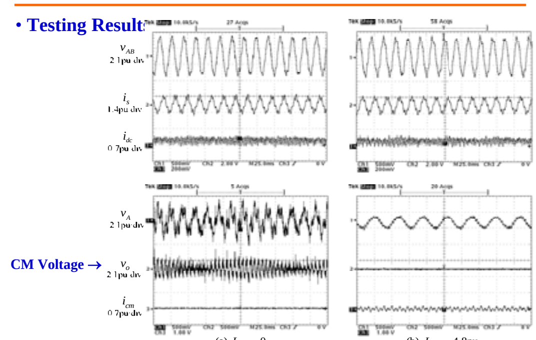
(a) Integrated dc choke

(b) Connection diagram

Common-mode voltage: v_o (motor neutral to GND)

Transformerless CSI Drives for Std Motors

• **Testing Result**

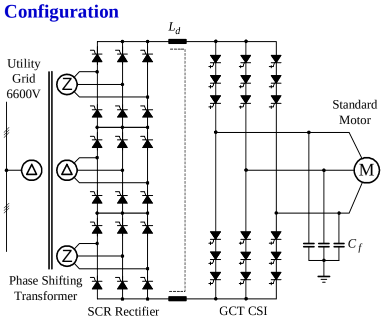


(a) $L_{cm} = 0$
Without CM inductance

(b) $L_{cm} = 4.8$pu
With CM inductance

CSI Drive With SCR Rectifiers

• **Drive Configuration**



Summary

• **Features and Drawbacks of MVCSI Drives**

Features
- **Simple converter structure with component count**
- **Motor friendly waveforms**
- **Reliable fuseless short circuit protection**
- **N+1 provision for high reliability**
- **Regenerative braking capability**
- **Inherent four quadrant operation**

Drawbacks
- **Limited dynamic performance**
- **Potential LC resonances**

Summary - MV Industrial Drives

Inverter Configuration	Switching Device	Power Range	Manufacturer
Two-Level Voltage Source Inverter	IGBT	1.4MVA – 7.2MVA	Alstom (VDM5000)
Three-Level Neutral Point Clamped Inverter	GCT	0.3MVA – 5MVA 3MVA – 27MVA	ABB (ACS1000) (ACS6000)
	GCT	3MVA – 20MVA	General Electric (Innovation Series MV-SP)
	IGBT	0.6MVA – 7.2MVA	Siemens (SIMOVERT-MV)
	IGBT	0.3MVA – 2.4MVA	General Electric–Toshiba (Dura-Bilt5 MV)
Multilevel Cascaded H-Bridge Inverter	IGBT	0.3MVA – 22MVA	ASI Robicon (Perfect Harmony)
		0.5MVA – 6MVA	Toshiba (TOSVERT-MV)
		0.45MVA – 7.5MVA	General Electric (Innovation MV-GP Type H)
NPC/H-bridge Inverter	IGBT	0.4MVA – 4.8MVA	Toshiba (TOSVERT 300 MV)
Flying-Capacitor Inverter	IGBT	0.3MVA – 8MVA	Alstom (VDM6000 Symphony)
PWM Current Source Inverter	Symmetrical GCT	0.2MVA – 20MVA	Rockwell Automation (PowerFlex 7000)
Load Commutated Inverter	SCR	>10MVA	Siemens (SIMOVERT S)
		>10MVA	ABB (LCI)
		>10MVA	Alstom (ALSPA SD7000)

High-Power Converters and AC Drives