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## Faculty of Engineering and Architectural Science

Department of Electrical and Computer Engineering

**EE8506: Digital CMOS VLSI Integrated Circuits**

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**Prerequisites**  None

**Course Web Page**  Course website on Blackboard (<http://my.ryerson.ca>)

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| **Compulsory Texts:** | | 1. Neil H. E. Weste and David Harris, *CMOS VLSI Design: A Circuit and Systems Perspective,* Addison-Wesley, 2011. (ISBN-13: 978-0-321-54774-3) 2. Laboratory manual: *ELE734 Low Power Digital Integrated Circuits Laboratory Manual,* Ryerson University. |
| **Reference**  **Texts:** | | None |
| **Calendar Description** | | This course deals with the design of Digital CMOS integrated circuits. The course consists of three essential components: Theory, Laboratory, and project. Variety of design techniques, such as Static CMOS, Dynamic CMOS, and Transmission Gate are discussed in theory. These designs are studied on basic logic gates as well as combinational and sequential circuits. The lessons learned are applied to arithmetic building blocks such as adders, multipliers, and memory elements. A MOS transistor is studied using I-V equations, and the different areas of operations are modeled. The static (DC) are dynamic (transient) behaviors for an important building block, a CMOS inverter, are studied in depth. |
| **Learning Objectives** | | |  | | --- | | At the end of this course, the successful student will have a solid understanding of the operations of MOS transistors pertaining to digital circuit operations including the I-V characteristics of MOS transistors, static and dynamic behaviours of the CMOS inverter, Static CMOS design techniques, Dynamic CMOS design techniques, Transmission Gate design techniques, and the performance and power evaluation of digital CMOS circuits. The student will develop a good understanding of the basic logic gate design techniques as well as advanced combinational and sequential circuit design techniques including the design and implementation of arithmetic building blocks such as adders, multipliers, and memory elements. The student will also be able to perform schematic-level and layout-level design of advanced digital CMOS circuits using computer-aided design tools (CAD) from Cadence Design Systems (CAD tools for IC design are used extensively in both laboratories and course projects). | |  | |
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| **Course Organization** | | 3 hours of lecture per week for 13 weeks  2 hours of lab per week for 12 weeks |
| **Course Evaluation** | Midterm exam 20%  Labs 30%  Course Project 20%  Final exam 30%  Total 100%  To achieve a passing grade, student must pass both the theory and laboratory/project components. | |
| **Examinations** | Midterm examination is a 1.5-hour, closed-book examination with one page of aid-sheet that covers all the lecture and laboratory materials up to the week of mid-term examination.  Final examination is a 3-hour closed-book examination with two pages of aid-sheet that covers all the course material and laboratory materials. | |
| **Project** | Students are required to perform the design and layout of either a 4x4 array multiplier or an 8 entry SRAM block using a given CMOS technology and CAD tools from Cadence Design Systems. The design of the system must contain the followings: (i) Schematic-level design - The schematic-level design must be fully simulated to verify its correctness. All schematics of the design must be included in the project report. The dimensions of all transistors and devices must be tabulated explicitly and included in the project report. All simulation results must be included in the project report. The critical path(s) of the circuit must be correctly identified. The performance of the critical path(s) must be measured through simulation. Reasonable effort must be made to minimize the delay of the critical path(s). (ii) Layout-level design – the layout-level design must faithfully reproduce the schematic-level design decisions that are made in (i). Efforts must be made to produce a modular and regular layout in order to minimize layout effort. (iii) Layout Vs Schematic (LVS) comparison and the measured performance of the post layout critical path(s) through simulation. (iv) Project reports must be prepared in a single-column double-space format, and must contain the followings:   * + Title page - Title of the project, authors' name, and course name.   + Abstract - Abstract of the project report.   + Table of contents - list of chapters, sections, and subsections of the project report.   + List of figures - list of all figures in the project report.   + List of tables - list of all tables in the project report.   + Main body of the project report - All schematics and figures must be embedded in the main body of the report and numbered.   + References - list of the books, journal papers, conference papers, and other publications used in the project report. References must be listed using IEEE reference styles. You need to take a look at *IEEE Transactions on Circuits and Systems I - Regular Papers* and *IEEE Journal of Solid-State Circuits* for IEEE reference styles on books, journal papers, conference papers, and technical reports.   + Appendices   + Index - list of key words and their page number in the project report. | |

**Course Content**

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| Week | Detailed Description | Hours |
| 1 | Introduction to Digital CMOS Design | 3 |
| 2 | MOS Transistor Theory | 3 |
| 3 | Circuit Simulation | 3 |
| 4-5 | Delay Estimation | 4.5 |
| 5-6 | Power Estimation | 4.5 |
| 7-8 | Interconnect Design (Midterm in week 8) | 4 |
| 9-10 | Combinational Circuit Design | 4.5 |
| 10-11 | Datapath Subsystems | 4.5 |
| 12-13 | Sequential Circuit Design | 4.5 |
| 13 | Review and Catch-up | 1.5 |

**Laboratory/Projects - Room ENG408**

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| **Labs.** | **Detailed Description** | **Week** |
| 1 | Lab 1: Characteristics of MOSFET Devices | 2-4 |
| 2 | Lab 2: CMOS Inverter Design | 5-7 |
| 3 | Lab 3: CMOS Logic Families | 8-10 |
| 4 | Lab 4: 1-bit CMOS Full Adder | 11-13 |
| Project | Students are required to perform the design and layout of either an 4x4 array multiplier or an 8 entry SRAM block using a given CMOS technology and CAD tools from Cadence Design Systems. |  |

**Note:** Schedule of lectures and labs is tentative. There may be some changes in the schedule that will be announced in the class and posted on course website.

**Important Notes**

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| 1. All of the required course-specific written reports will be assessed not only on their technical/academic merit, but also on the communication skills exhibited through these reports. 2. All assignment and lab/tutorial reports must have the standard cover page which can be completed and printed from the Department website at www.ee.ryerson.ca. The cover page must be signed by the student(s) prior to submission of the work. Submissions without the cover pages **will not** be accepted. |

3. Should a student miss a mid-term test or equivalent (e.g. studio or presentation), with appropriate documentation, a make-up will be scheduled as soon as possible in the same semester. Make-ups should cover the same material as the original assessment but need not be of an identical format. Only if it is not possible to schedule such a make-up may the weight of the missed work be placed on the final exam, or another single assessment. This may not cause that exam or assessment to be worth more than 70% of the student’s final grade. If a student misses a scheduled make-up test or exam, the grade may be distributed over other course assessments even if that makes the grade on the final exam worth more than 70% of the final grade in the course.

4. Students who miss a final exam for a verifiable reason and who cannot be given a make-up exam prior to the submission of final course grades, must be given a grade of INC (as outlined in the *Grading Promotion and Academic Standing Policy)* and a make-up exam (normally within 2 weeks of the beginning of the next semester) that carries the same weight and measures the same knowledge, must be scheduled.

5. Medical or Compassionate documents for the missing of an exam must be submitted within 3 working days of the exam. Students are responsible for notifying the instructor that they will be missing an exam as soon as possible.

6. Requests for accommodation of specific religious or spiritual observance must be presented to the instructor no later than two weeks prior to the conflict in question (in the case of final examinations within two weeks of the release of the examination schedule). In extenuating circumstances this deadline may be extended. If the dates are not known well in advance because they are linked to other conditions, requests should be submitted as soon as possible in advance of the required observance. Given that timely requests will prevent difficulties with arranging constructive accommodations, students are strongly encouraged to notify the instructor of an observance accommodation issue within the first two weeks of classes.

7. The results of the first test or mid-term exam will be returned to students before the deadline to drop an undergraduate course in good Academic Standing.

8. Students are required to adhere to all relevant University policies including:

Undergraduate Grading, Promotion and Academic Standing, <http://www.ryerson.ca/senate/policies/pol46.pdf>

Student Code of Academic Conduct, <http://www.ryerson.ca/senate/policies/pol60.pdf>

Student Code of Non-Academic Conduct, <http://www.ryerson.ca/senate/policies/pol61.pdf>

Undergraduate Academic Consideration and Appeals, <http://www.ryerson.ca/senate/policies/pol134.pdf>

Examination Policy, <http://www.ryerson.ca/senate/policies/pol135.pdf>

Accom. of Student Relig., Abor. and Spir. Observance, <http://www.ryerson.ca/senate/policies/pol150.pdf>

Est. of Stud. Email Accts for Official Univ. Commun., <http://www.ryerson.ca/senate/policies/pol157.pdf>

9. Students are required to obtain and maintain a Ryerson Matrix e-mail account for timely communications between the instructor and the students.

10. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented.

11. In-class use of cellular telephones is not permitted. Please turn off your cell phone prior to class. Quiet use of laptops, text-messengers and similar non-audible devices are permitted only in the rear rows of the class. This restriction allows use of such devices by their users while limiting audible and visual distractions to other students. This policy may change without notice.

12. Labs, projects handed in past the due date and time will not be accepted for marking and will receive a mark of ZERO. In some genuine cases late submission will be allowed with a penalty of 5% per day.

13. Students found to have plagiarized *any* portion of their labs and final project will receive a grade of zero on the *complete* project. This automatically will lead to a failing grade

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| Name of Instructor |  | Signature of Instructor |  | Date |  |
| Name of Graduate Program Director |  | Signature of Graduate Program Director |  | Date |  |