Course Title:
Field-Programmable Gate Array Architectures

Course Description:
This course will explore various aspects in the design of Field-Programmable Gate Arrays (FPGAs). FPGAs are a class of digital devices that enable the rapid prototyping and implementation of digital systems. Comparing to traditional methods of implementing digital applications, FPGAs combine the programmability of CPU systems with the ability of exploring the massive amount of parallelism inherent in many digital applications. As the logic capacity and application domain of FPGAs grow, their design has become increasingly complex and requires specialized engineering expertise. This course will explore the design of FPGA devices from an architectural perspective. We will exam a wide range of FPGA architectures and discuss the various methods employed in the modelling and evaluation of these architectures. The particular topics that will be covered in this course include:

1. The Modelling and Evaluation of FPGA Architectures
2. High-Level CAD Algorithms used in FPGA Architectural Evaluation – Technology Mapping and Packing Tools
3. Physical-Level CAD Algorithms used in FPGA Architectural Evaluation – Placement and Routing Tools
4. Power Modelling and Power-Aware CAD Tools for FPGAs
5. Low Power FPGA Architectures and Circuit-Level Design Techniques

Prerequisites:
Knowledge of digital hardware design and C programming and at least one of the following courses: ELE734 (Low-Power Digital Integrated Circuits), ELE863 (VLSI Systems), EE8501 (VLSI System Design), or EE8504 (VLSI Design Automation and CAD Tools).

Course Text:
Architecture and CAD for Deep-Submicron FPGAs, Vaughn Betz, Jonathan Rose, and Alexander Marquardt, Kluwer Academic Publishers, 1999, ISBN: 0-7923-8460-1

Reference Material: Research papers will be suggested as the course proceeds.

Assignments and Tests:
The course will consist of three homework assignments, a midterm test and a final project. The homework assignments will cover the following three areas:

1. A Survey of Commercial FPGA Architectures (10%)
2. FPGA Architecture Modelling and Evaluation (10%)
3. Design and Tuning of FPGA CAD Tools (10%)

The project will consist of a specific FPGA architectural modelling and evaluation assignment chosen by the instructor or a project of equivalent difficulty chosen by the student in the area of FPGA architecture and CAD design.

Evaluation:

Assignments:	30%
Project:	30%

Final Exam: 35%
Class Participation: 5%

Course Outline:

Week 1: Course Management, Introduction to FPGAs, FPGA Programming Technologies
Week 2: The Evolution of FPGA Logic Block Architectures (*Start of Assignment 1*)
Week 3: The Evolution of FPGA Routing Architectures
Week 4: Cluster-Based FPGA Logic Blocks and Packing Algorithms (Technology mapping and look-up tables, clustering) (**Assignment 1 Due**) (*Start of Assignment 2*)
Week 5: FPGA Placement Algorithms (Simulated Annealing, Force Directed, or Quadratic)
Week 6: Routing Tools Part I (**Assignment 2 Due**) (*Start of Assignment 3*)
Week 7: Routing Tools Part II
Week 8: FPGA Circuitry and Process Modelling I: Circuitry and Area Modelling (**Assignment 3 Due**) (*Start of Project*)
Week 9: FPGA Process Modelling II: Delay Modelling and the Sizing of Routing Transistors and Metal
Week 10: Power Modelling Techniques for FPGAs
Week 11: Power Efficient Circuitry and Architectures for FPGAs I
Week 12: Power Efficient Circuitry and Architectures for FPGAs II
Week 13: Final Exam
Week 14: **Project Due**