

Course Outline (W2026)

ELE863: VLSI Circuits for Data Communications

Instructor(s)	Dr. Fei Yuan [Coordinator] Office: ENG-433 Phone: (416) 979-5000 x 556100 Email: fyuan@torontomu.ca Office Hours: Friday 1-4 pm via ZOOM (ID. 925 1090 3365, Passcode : ELE827-863)
Calendar Description	An advanced course on design of VLSI circuits for data communications over wire channels. The theoretical component consists of: switching noise and grounding of mixed analog-digital circuits, modeling of wire channels, clock generation and distribution, power distribution on chip, ESD protection, channel equalization, clock and data recovery. The laboratory component consists of design of clock and data recovery circuits using state-of-the-art CMOS technology and CAD tools.
Prerequisites	ELE 727 or ELE 734
Antirequisites	None
Corerequisites	None
Compulsory Text(s):	<ol style="list-style-type: none"> 1. ELE 863 Lecture Notes from Dr. Fei Yuan (available from D2L). 2. Laboratory manual: ELE 863 Laboratory Manual (available from D2L).
Reference Text(s):	<ol style="list-style-type: none"> 1. B. Razavi, Design of Integrated Circuits for Optical Communications, McGraw-Hill, 2003 2. H. Johnson and M. Graham, High-speed digital design - A handbook of black magic, Prentice-Hall, 1993. 3. Stojanovic, Channel-limited high-speed links: modeling, analysis and design, PhD Dissertation, Stanford University, 2004. 4. Published peer-reviewed scientific papers in scientific journals and conference proceedings.
Learning Objectives (Indicators)	<p>At the end of this course, the successful student will be able to:</p> <ol style="list-style-type: none"> 1. Improve their capabilities of using the technical knowledge of VLSI circuits to design a transceiver for data communications. (4b) 2. Utilize computer-aided design tools for integrated circuit design to iteratively design a transceiver for data communications over wire channels. (4c) 3. Proficiency in use of computer-aided design tools from Cadence Design Systems for integrated circuit design to design and analyze a transceiver for data communications over wire channels. (5a) 4. Write professionally prepared laboratory reports. Laboratory reports are evaluated on their correctness, completeness, English, and quality of graphics. (7a), (7c) <p>NOTE: Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).</p>

Course Organization	3.0 hours of lecture per week for 13 weeks 2.0 hours of lab per week for 12 weeks 0.0 hours of tutorial per week for 12 weeks												
Teaching Assistants	1. Francisco Braga (francisco.braga@torontomu.ca) : Section 1 2. David Wu (wenhao.wu@torontomu.ca) : Sections 2/3												
Course Evaluation	<table border="1"> <thead> <tr> <th colspan="2">Theory</th> </tr> </thead> <tbody> <tr> <td>Midterm Exam</td> <td>30 %</td> </tr> <tr> <td>Final Exam</td> <td>30 %</td> </tr> <tr> <th colspan="2">Laboratory</th> </tr> <tr> <td>Lab Projects</td> <td>40 %</td> </tr> <tr> <td>TOTAL:</td> <td>100 %</td> </tr> </tbody> </table> <p>Note: In order for a student to pass a course, a minimum overall course mark of 50% must be obtained. In addition, for courses that have both "Theory and Laboratory" components, the student must pass the Laboratory and Theory portions separately by achieving a minimum of 50% in the combined Laboratory components and 50% in the combined Theory components. Please refer to the "Course Evaluation" section above for details on the Theory and Laboratory components (if applicable).</p>	Theory		Midterm Exam	30 %	Final Exam	30 %	Laboratory		Lab Projects	40 %	TOTAL:	100 %
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Examinations	1. 3-hour closed-book midterm exam during regular lecture time on Feb. 24. 2. 3-hour closed-book final exam during university exam period with date/time set by the university. Only course materials covered AFTER the midterm exam will be tested.												
Other Evaluation Information	None												
Other Information	None												

Course Content

Week	Hours	Chapters / Section	Topic, description
1-2			Module 1 - Modeling of wire channels 1) Components of wire channels 2) Scaling of wire channels 3) Resistance of wire channels 4) Capacitance of wire channels 5) Inductance of wire channels 6) Modeling of wire channels at low, intermediate, and high frequencies 7) Transmission-line effect

			8) Termination schemes
3			<p>Module 2 - Electrical signaling</p> <ol style="list-style-type: none"> 1) Single-ended signaling 2) Fully differential signaling 3) Pseudo-differential signaling 4) Voltage-mode incremental signaling 5) Current-mode signaling 6) Current-mode incremental signaling
3			<p>Module 3 - Fundamentals of serial links</p> <ol style="list-style-type: none"> 1) Data encoding for serial links 2) Data modulation for serial links 3) Eye diagrams 4) Inter-symbol interference 5) Bit-error rate 6) Test of serial links
4			<p>Module 4 - Pre-emphasis</p> <ol style="list-style-type: none"> 1) Channel equalization 2) Pre-emphasis strategies 3) Basic idea of pre-emphasis 4) Pre-emphasis algorithms 5) Pre-emphasis algorithms : A zero/pole perspective 6) Pre-emphasis algorithms : A frequency response perspective 7) Pre-emphasis waveforms 8) Implementation of pre-emphasis FIR filters 9) Advantages of pre-emphasis 10) Limitations of pre-emphasis
5			<p>Module 5 - Continuous-time linear equalization</p> <ol style="list-style-type: none"> 1) Channel impairments 2) Channel equalization 3) Continuous-time linear equalization 4) Continuous-time linear equalization - Source degeneration 5) Continuous-time linear equalization - Negative capacitors 6) Continuous-time linear equalization - Inductor shunt-peaking 7) Continuous-time linear equalization - Complete design
6			Mid-term examination during normal lecture time on Feb. 22.

7-9			<p>Module 6 Phase/frequency-locked loop</p> <ol style="list-style-type: none"> 1) Voltage-controlled ring oscillators 2) Noise 3) Spectrum (phase noise) of oscillators 4) Phase detectors 5) Charge pumps 6) Loop filters 7) Loop dynamics of type-1 phase-locked loops 8) Loop dynamics of type-2 phase-locked loops 9) Phase noise of phase-locked loops 10) All-digital phase-locked loops <ul style="list-style-type: none"> - TDC-based ADPLL - Delay line TDC - Delay-locked loops - Vernier TDC - Cyclic Vernier TDC - Digital phase interpolation - Digital loop filters (FIR, IIR filters) - Digital controlled oscillators (DCOs) 11) Frequency synthesizers <ul style="list-style-type: none"> - Injection-locked frequency dividers - DFF-based frequency dividers - Frequency difference detectors - Frequency-locking and phase-locking in frequency synthesizers
10-11			<p>Module 7 - Decision feedback equalization (DFE)</p> <ol style="list-style-type: none"> 7.1 Decision feedback equalization <ol style="list-style-type: none"> 1) Postcursor-induced ISI 2) Principle of DFE 3) Configuration of DFE 4) Characteristics of DFE 5) Challenges of DFE 6) DFE blocks 7.2 Adaptive decision feedback equalization <ol style="list-style-type: none"> 1) Classification of DFE 2) Data-state (DS) DFE 3) Data-transit (DT) DFE 4) Weighted DS-DFE and DT-DFE 5) Adaptive DFE 6) Least-mean-square (LMS) adaptive DFE algorithm 7) Sign-sign (S^2) LMS adaptive DFE algorithm 8) SS-LMS implementation 9) Error detection unit for adaptive DS-DFE 10) Reference voltages 11) Error detection unit for adaptive DT-DFE 12) Charge pumps and loop filters
12-13			<p>Module 8 - Clock and data recovery</p> <ol style="list-style-type: none"> 1) Clock recovery 2) Frequency drift of receiver PLL 3) Direct coupling and AC coupling 4) Data encoding 5) Classification of clock recovery 6) Clock recovery using phase tracking

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| | | | 7) Clock recovery using phase picking
8) Clock recovery using phase interpolation |
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Laboratory(L)/Tutorials(T)/Activity(A) Schedule

Week	L/T/A	Description
2/3	Lab 1	Wire channels. Report due : Sunday mid-night of Week 3 if your lab is in Week 2 and Sunday mid-night of Week 4 if your lab is in Week 3.
4/5	Lab 2	Pre-emphasis. Report due : Sunday mid-night of week 5 if your lab is in Week 4 and Sunday mid-night of Week 6 if your lab is in Week 5.
6/7	Lab 3	Continuous-time linear equalizer. CTLE report due : Sunday mid-night of week 7 if your lab is in Week 6 and Sunday mid-night of Week 8 if your lab is in Week 7.
8/9	Lab 4	Phase-locked loop. PLL report due : Sunday mid-night of week 9 if your lab is in Weeks 8 and Sunday mid-night of Week 10 if your lab is in Weeks 9.
10/11	Lab 5	Decision feedback equalizer. Report due : Sunday mid-night of week 11 if your lab is in Week 10 and Sunday mid-night of Week 12 if your lab is in week 11.
12/13	Lab 6	Clock and data recovery. Report due : Sunday mid-night of week 13.

University Policies & Important Information

Students are reminded that they are required to adhere to all relevant university policies found in their online course shell in D2L and/or on [the Senate website](#)

Refer to the [Departmental FAQ page](#) for further information on common questions.

Important Resources Available at Toronto Metropolitan University

- [The University Libraries](#) provide research [workshops](#) and individual consultation appointments. There is a drop-in Research Help desk on the second floor of the library, and students can use the [Library's virtual research help service](#) to speak with a librarian, or [book an appointment](#) to meet in person or online.
- [Student Life and Learning Support](#) offers group-based and individual help with writing, math, study skills, and transition support, as well as [resources and checklists to support students as online learners](#).

- You can submit an [Academic Consideration Request](#) when an extenuating circumstance has occurred that has significantly impacted your ability to fulfill an academic requirement. You may always visit the [Senate website](#) and select the blue radio button on the top right hand side entitled: Academic Consideration Request (ACR) to submit this request.

For Extenuating Circumstances, [Policy 167: Academic Consideration](#) allows for a once per semester ACR request without supporting documentation if the absence is less than 3 days in duration and is not for a final exam/final assessment. Absences more than 3 days in duration and those that involve a final exam/final assessment, always require documentation. Students must notify their faculty/contract lecturer once a request for academic consideration is submitted. See Senate [Policy 167: Academic Consideration](#).

Longer absences are not addressed through Policy 167 and should be discussed with your Chair/Director/Program to be advised on next steps.

- [FAQs Academic Considerations and Appeals](#)
- Information on Copyright for [Faculty/Contract Lecturers](#) and [students](#).

Lab Safety (if applicable)

Students are to strictly adhere and follow:

- a. The Lab Safety information/guidelines posted in the respective labs,
- b. provided in their respective lab handouts, and
- c. instructions provided by the Teaching Assistants/Course instructors/Technical Staff.

During the lab sessions, to avoid tripping hazards, the area around the lab stations should not be surrounded by bags, backpacks etc, students should place their bags, backpacks etc against the walls of the labs and/or away from their lab stations in such a way that it avoids tripping hazards.

Accessibility

- Similar to an [accessibility statement](#), use this section to describe your commitment to making this course accessible to students with disabilities. Improving the accessibility of your course helps minimize the need for accommodation.
- Outline any technologies used in this course and any known accessibility features or barriers (if applicable).
- Describe how a student should contact you if they discover an accessibility barrier with any course materials or technologies.

Academic Accommodation Support

Academic Accommodation Support (AAS) is the university's disability services office. AAS works directly with incoming and returning students looking for help with their academic accommodations. AAS works with any student who requires academic accommodation regardless of program or course load.

- Learn more about [Academic Accommodation Support](#).
- Learn [how to register with AAS](#).
- Learn about [Policy 159: Academic Accommodation of Students with Disabilities](#)

Academic Accommodations (for students with disabilities) and Academic Consideration (for students faced with extenuating circumstances that can include short-term health issues) are governed by two different university policies. Learn more about [Academic Accommodations versus Academic Consideration and how to access each](#).

Wellbeing Support

At Toronto Metropolitan University, we recognize that things can come up throughout the term that may interfere with a student's ability to succeed in their coursework. These circumstances are outside of one's control and can have a serious impact on physical and mental well-being. Seeking help can be a challenge, especially in those times of crisis.

If you are experiencing a mental health crisis, please call 911 and go to the nearest hospital emergency room. You can also access these outside resources at anytime:

- **Distress Line:** 24/7 line for if you are in crisis, feeling suicidal or in need of emotional support (phone: 416-408-4357)
- **Good2Talk:** 24/7-hour line for postsecondary students (phone: 1-866-925-5454)
- **Keep.meSAFE:** 24/7 access to confidential support through counsellors via [My SSP app](#) or 1-844-451-9700

If non-crisis support is needed, you can access these campus resources:

- **Centre for Student Development and Counselling:** 416-979-5195 or email csdc@torontomu.ca
- **Consent Comes First - Office of Sexual Violence Support and Education:** 416-919-5000 ext 3596 or email osvse@torontomu.ca
- **Medical Centre:** call (416) 979-5070 to book an appointment

We encourage all Toronto Metropolitan University community members to access available resources to ensure support is reachable. You can find more resources available through the [Toronto Metropolitan University Mental Health and Wellbeing](#) website.