Toronto Metropolitan University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Outline (F2022)

COE758: Digital Systems Engineering

Instructor(s)	Dr. Lev Kirischian [Coordinator] Office: ENG432 Phone: (416) 979-5000 x 556076 Email: lkirisch@ryerson.ca Office Hours: TBA
Calendar Description	The emphasis of this course is an understanding of the system architecture around the processor. Course covers all types of modern semiconductor memory, cache and virtual memory organization, hard disk drives and video-output subsystem. Course gives classification of buses and description of concepts of bus organization, bus protocols, arbitration mechanisms and the concept of Direct Memory Access (DMA). The laboratory projects include design of Cache Controller and VGA-signal generator using VHDL in Xilinx CAD environment.
Prerequisites	(COE 538 or ELE 538) and COE 608
Antirequisites	None
Corerequisites	None
Compulsory Text(s):	1. David Patterson and John Hennessy, “Computer Organization and Design: The hardware /Software Interface”, 5-th edition, Morgan Kaufmann Publishers Inc., San Francisco, CA USA, ISBN-9780124077263 2. Marilyn Wolf, "Computers as Components: Principles of Embedded Computing System Design", Fourth Edition, Morgan Kaufmann is an imprint of Elsevier, Cambridge, MA 02139, United States USA, ISBN: 978-0-12-805387-4 3. Vincent Heuring and Harry Jordan, “Computer Systems Design and Architecture”, Second edition, Prentice Hall, Pearson Education Inc., NJ, 07458, ISBN 0-13-048440-7
Reference Text(s):	1. https://www.ee.ryerson.ca/~lkirisch/coe758/handouts.htm
Learning Objectives (Indicators)	At the end of this course, the successful student will be able to: 1. Understand the concepts of memory hierarchy organization and be able to apply this knowledge for the design of major architectural components of modern computer systems: cache memory, cache and main memory controllers, virtual memory elements and associated hardware/software drivers. Describe principles of interfacing the processor with different types of Input / Output (I/O) devices, estimate bus bandwidth, select the most effective bus organization and design I/O device controllers & adapters for modern computer systems. (**4a**) 2. Describe principles of interfacing the processor with different types of Input / Output (I/O) devices, estimate bus bandwidth, select the most effective bus organization and design I/O device controllers & adapters for modern computer systems. Learn modern integrated CAD tools (e.g. Xilinx ISE) and Hardware Description Languages (e.g. VHDL) and apply the principles of on-chip hardware design: including symbol creation, top-bottom design, high-level synthesis of IP-core architecture for designing the on-chip (FPGA-based) IP-cores for

cache controllers, main memory interfaces, I/O device controllers and interfaces to real-time peripheral devices. (**4b**)
3. Integrate the on-chip (FPGA-based) IP-cores with the host computer and real-time peripheral device (e.g. SVGA video-display) and adjust timing parameters of the designed on-chip device controller. (**4c**)
4. Utilize the on-chip debugging techniques for modern FPGA-based hardware platforms (e.g. Xilinx Spartan FPGA devices), including synthesis and application of the on-chip test-vector generators, utilization of on-chip logic analyzers (e.g. Xilinx ChipScope), creation of the hardware emulation environment and systematic analysis of timing diagrams received from the on-chip logic analyzers. (**5a**)
5. Produce project reports using appropriate format of technical reports, grammar, and citation styles for technical and non-technical audiences. (**7a**)
6. Illustrate concepts including the structure of IP-cores VHDL-code with appropriate comments and obtained experimental results. (**7c**)

NOTE:*Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).*

Course Organization

3.0 hours of lecture per week for 13 weeks
2.0 hours of lab per week for 12 weeks
0.0 hours of tutorial per week for 12 weeks

Teaching Assistants

1. Tajinderpal Toor;
2. Parastoo Seyed Jafarzadeh Hesar.

Course Evaluation

Theory	
Midterm Exam	25 %
Final Exam	45 %
Laboratory	
Tutorials	2 %
Lab Project 1	14 %
Lab Project 2	14 %
TOTAL:	100 %

Note: In order for a student to pass a course, a minimum overall course mark of 50% must be obtained. In addition, for courses that have both **"Theory and Laboratory"** components, the student must pass the Laboratory and Theory portions separately by achieving a minimum of 50% in the combined Laboratory components and 50% in the combined Theory components. Please refer to the **"Course Evaluation"** section above for details on the Theory and Laboratory components (if applicable).

Examinations

Midterm exam in Week 8, two hours, closed book, problem solving (covers Weeks 1-6).
Final exam, three hours, closed-book, problem solving (covers all course material).

Other Evaluation Information

The laboratory projects include design of IP-cores of custom on-chip modules for cache controller and video-signal generator for SVGA-monitor. Both projects include all major stages of on-chip design of custom digital systems: coding on VHDL hardware description language, compilation and design evaluation in Xilinx ISE CAD environment and hardware implementation on Xilinx Spartan FPGA platform.
In case of virtual lab project, the hardware implementation may be replaced by functional simulation procedures and analysis.

	In assigned projects students are required to develop the custom IP-cores on the base of Xilinx Spartan FPGA development platform. The goal is to apply the theoretical knowledge to on-chip system design and get practical experience in VHDL-coding, simulation and on-chip verification of the designed module (in case of virtual lab project, on-chip hardware verification may be skipped). There are two projects associated with different aspects of the system-on-chip (SoC) design: 1) IP-core design of the control-dominated circuit (Project 1: Cache Controller) and 2) IP-core design of the data-path dominated circuit (Project 2: Video-signal generator). For both projects the requirements are to demonstrate ability to create symbol of the system, develop system block-diagram, write the VHDL-code, compile and simulate it in Xilinx CAD environment, verify the behaviour on the Xilinx Spartan FPGA development platform using on-chip instrumentation (Chip-Scope), demonstrate the complete IP-core performance and submit the project report. Additionally, Project 2 requires integration the FPGA platform with the real-time I/O device (SVGA video-monitor) and demonstrate working project in all modes of operation (if lab facilities are available). Lab Management The Completed tutorials accounts to 2% and Lab Projects accounts for 14% each of the final mark. Each project must be demonstrated during the demonstration week. The project report must be submitted after successful project demonstration before the end of the demonstration week. The detailed evaluation of Lab components and projects is as follows: 1. 2% - Completed tutorials 2. 14% for each project: 2% - Symbol & block diagram design 3% - Compiled VHDL code demonstration 4% - Complete project demonstration on the FPGA platform 5% - Project report All the tutorials and projects could be done individually or in group of 2 students. Equipment should not be moved before during or after the lab. In case if equipment seems to be defective it is a requirement to report to the lab instructor / technician who will take care of the problem.
Teaching Methods	The teaching method is based on: a) presentation the theory component in in-person lectures using the white board and slides; b) recommendation self-learning materials: text book chapters and lab tutorials and c) implementation of the theory in the associated lab projects to provide practical hands-on experience in system-on-chip (SoC) design and functional verification using a) on-chip verification tools (e.g. Xilinx Chip-Scope) and platform tools (e.g. Logic Analysers, video-monitors, etc.).
Other Information	In case of on-line course re-presentation, lectures are provided in form of prerecorded mp4 video-files to be viewed on D2L platform. Questions regarding each lecture should be sent via e-mail. Answers may be provided individually via e-mail communication or via Zoom meeting session. In case of on-line project performance and demonstration, hardware implementation on the FPGA platform is skipped and replaced by software simulation. Therefore, complexity of the projects became different and Project 1 is accounted for 16% of total mark and Project 2 is 12% accordingly.

Course Content

Week	Hours	Chapters / Section	Topic, description
1	3	B1: Ch.5/ 5.1	1. Introduction to COE 758: Scope and Objectives Management.

			2. Memory hierarchy and types of memory elements and their organization Read Book 1 Chapter 5 section 5.1 pp. 374-378 Book 2 Chapter 4 section 4.4 pp. 177-181 Book 3 Chapter 7 section 7.1 pp. 304-309
2	3	B1: Ch 5/ 5.2	Types of electronic memory and their organization: 1. Static and Dynamic Random Access Memory (RAM) structure and timing 2. Main memory components: DRAM EDO-DRAM SDRAM DDR-SDRAM RDRAM: structure, interface,timing Read Book 1 Chapter 5 section 5.2 pp. 378-383 Book 3 Chapter 7 section 7.2 pp. 309-325
3	3	B1: Ch 5/ 5.3	Cache memory organization: 1. Principles of locality concepts terminology and organization of cache 2. Direct mapped cache: principles of operation and cache performance 3. Handling cache misses and writes. Cache & main memory coherence. Read Book 1 Chapter 5 section 5.3 pp. 383-398 Book 2 Chapter 3 section 3.5.1 pp. 119-126 Book 3 Chapter 7 section 7.4 pp. 340-345
4	3	B1: Ch 5/ 5.4	Associative cache memory organization: 1. Ping-pong effect in direct mapped cache and cache efficiency 2. Two-way associative cache memory organization and operation 3. N-way associative cache: principles of operation pros and cons 4. Multi-level cache: concept organization and performance. Read Book 1 Chapter 5 section 5.4 pp. 398-413
5	3	B1: Ch 5/ 5.7	Virtual memory: concept and organization: 1. Concept of memory virtualization terminology and general organization 2. Address translation page table and page replacement mechanism. Read Book 1 Chapter 5 section 5.7 pp. 427-437 Book 2 Chapter 3 section 3.5.2 pp. 126-131 Book 3 Chapter 7 section 7.6 pp. 355-360
6	3	B1: Ch 5/ 5.7	Virtual memory: concept and organization: 1. Fast address translation in Translation Look aside Buffer (TLB) 2. Integrating virtual memory: TLB+cache+main memory+secondary storage. Read Book 1 Chapter 5 section 5.7 pp. 438-453 Book 3 Chapter 7 section 7.6 pp. 361-365
7	2	B1: Ch 5 / 5.1 - 5.8	Midterm test: Preparation read: Book 1 Chapter 5 section 5.8 pp. 454-461
8	3	B3 Ch 8 / 8.1-8.3	Input-Output (I/O) subsystem organization: 1. Typical set of I/O devices in computing system 2. Interfacing processor(s) to I/O devices Read Book 3 Chapter 8 sections 8.1-8.3 pp. 371-393

9	3	B3 Ch 9 / 9.1-9.3	Secondary data-storage devices: 1. Hard Disc Drive (HDD) principles of operation and performance 2. Solid State Drive (SSD) principles of operation and performance. Read Book 3 Chapter 9 sections 9.1-9.2 pp. 407-420
10	3	B3 Ch 9 / 9.4	Video-output subsystem organization: 1. Video-displays: principles of operation in graphical and character modes 2. Video-adaptors and video-processors: principles of operation and timing. Read Book 3 Chapter 9 section 9.4 pp. 421-429
11	3	B2 Ch 4 / 4.2	Buses: 1. Classification of buses synchronization and handshaking 2. Synchronous and asynchronous buses. Bus protocols and timing 3. Bus bandwidth calculation and methods for acceleration. Read Book 2 Chapter 4 section 4.3.1 pp. 165-171
12	3	B2 Ch 4 / 4.2	Bus arbitration and multi-level buses: 1. Bus arbitration mechanisms: Daisy-chain and centralized arbitration 2. Multi-level buses: Integration the memory bus and I/O buses 3. Direct memory Access (DMA): principles of operation and transfer modes. Read Book 2 Chapter 4 section 4.3.2 pp. 171-177 Book 3 Chapter 8 section 8.4 pp. 393-396
13	2	B3 Ch 8 /	Interaction between CPU I/O devices and memory: 1. Giving commands to I/O devices 2. Interrupt priority levels and interrupt service routines 3. Process of data transferring between CPU memory and I/O device. Book 3 Chapter 8 section 8.3 pp. 386-393
13	1		Review and Catch-up

Laboratory(L)/Tutorials(T)/Activity(A) Schedule

Week	L/T/A	Description
2	Tutorial	Introduction to Xilinx ISE CAD and FPGA development environment Reference tutorial: https://www.ee.ryerson.ca/~lkirisch/ele758/handouts/Tutorial1_ISE_Project_Creation.pdf

3	Project 1 Spec.	Tutorials: Design components in Xilinx Spartan FPGA. Project 1 Specification Reference tutorials: https://www.ee.ryerson.ca/~lkirisch/ele758/handouts/COE758_Digital_Design_Tutorial.pdf https://www.ee.ryerson.ca/~lkirisch/ele758/labs/Cache%20Project[12-09-10].pdf Read Book 1 Chapter 5 section 5.9 pp. 461-466
4	Project 1 Symbol	Creation of the symbol and block diagram of the Cache Controller SoC
5-6	Project 1 VHDL	VHDL-coding and compilation. Creation of simulation/hardware emulation environment and verification
7	Project 1 Demo	Complete project 1 demonstration and report submission
8	Project 2 Spec.	Introduction to video-processing systems and Project 2 specification
9	Project 2 Symbol	Creation of the symbol and block diagram of the Video-Game Processor SoC
10-11	Project 2 VHDL	VHDL-coding and compilation. Creation of simulation environment and verification
12	Project 2 Demo	Complete project 2 demonstration and report submission

Policies & Important Information:

Students are reminded that they are required to adhere to all relevant university policies found in their online course shell in D2L and/or on the Senate website

1. In accordance with the Policy on TMU Student E-mail Accounts (Policy 157), Toronto Metropolitan University (TMU) **requires** that any electronic communication by students to TMU faculty or staff be sent from their official university email account;
2. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented;
3. Assignments, projects, reports and other deadline-bound course assessment components handed in past the due date will receive a mark of ZERO, unless otherwise stated. Marking information will be made available at the time when such course assessment components are announced.
4. Familiarize yourself with the tools you will need to use for remote learning. The Continuity of Learning Guide for students includes guides to completing quizzes or exams in D2L or Respondus, using D2L Brightspace, joining online meetings or lectures, and collaborating with the Google Suite.
5. The University has issued a minimum technology requirement for remote learning. Details can be found at: https://torontomu.ca/covid-19/students/minimum-technology-requirements-remote-learning. Please ensure you meet the minimum technology requirements as specified in the above link.
6. Toronto Metropolitan University COVID-19 Information and Updates (available https://www.torontomu.ca/covid-19/students) for Students summarizes the variety of resources available to students during the pandemic.

7. Refer to our **Departmental FAQ** page for information on common questions and issues at the following link: https://www.ecb.torontomu.ca/guides/Student.Academic.FAQ.html.

Missed Classes and/or Evaluations

When possible, students are required to inform their instructors of any situation which arises during the semester which may have an adverse effect upon their academic performance, and must request any consideration and accommodation according to the relevant policies as far in advance as possible. Failure to do so may jeopardize any academic appeals.

1. **Academic Consideration Requests for missed work** (e.g. missing tests, labs, etc) - According to Senate Policy 134, Section 1.2.3, if you miss any exams, quizzes, tests, labs, and/or assignments for health or compassionate reasons you need to inform your instructor(s) (via email whenever possible) in advance when you will be missing an exam, test or assignment deadline. When circumstances do not permit this, you must inform the instructor(s) as soon as reasonably possible". *In the case of illness, a Toronto Metropolitan Student Health Certificate, or a letter on letterhead from an appropriate regulated health professional with the student declaration portion of the Student Health Certificate attached. For reasons other than illness, proper documentation is also required (e.g. death certificate, police report, TTC report).* ***ALL supporting documentation for illness or compassionate grounds MUST be submitted within three (3) working days of the missed work.*** " **NOTE: You are required to submit all of your pertinent documentation through the University's online Academic Consideration Request system at the following link:** prod.apps.ccs.ryerson.ca/senateapps.
2. ***Religious, Aboriginal and Spiritual observance*** - If a student needs accommodation because of religious, Aboriginal or spiritual observance, they must submit a Request for Accommodation of Student Religious, Aboriginal and Spiritual Observance AND an Academic Consideration Request form within the first 2 weeks of the class or, for a final examination, within 2 weeks of the posting of the examination schedule. If the requested absence occurs within the first 2 weeks of classes, or the dates are not known well in advance as they are linked to other conditions, these forms should be submitted with as much lead time as possible in advance of the absence. Both documents are available at www.torontomu.ca/senate/forms/relobservforminstr.pdf. **If you are a full-time or part-time degree student, then you submit the forms to your own program department or school;**
3. ***Academic Accommodation Support*** - Before the first graded work is due, students registered with the Academic Accommodation Support office (AAS - prod.apps.ccs.ryerson.ca/senateapps) should provide their instructors with an Academic Accommodation letter that describes their academic accommodation plan.

Virtual Proctoring Information (if used in this course)

Online exam(s) within this course may use a virtual proctoring system. Please note that your completion of any such virtually proctored exam may be recorded via the virtual platform and subsequently reviewed by your instructor. The virtual proctoring system provides recording of flags where possible indications of suspicious behaviour are identified only. Recordings will be held for a limited period of time in order to ensure academic integrity is maintained and then will be deleted.

Access to a computer that can support remote recording is your responsibility as a student. The computer should have the latest operating system, at a minimum Windows (10, 8, 7) or Mac (OS X 10.10 or higher) and web browser Google Chrome or Mozilla Firefox. You will need to ensure that you can complete the exam using a reliable computer with a webcam and microphone available, as well as a typical high-speed internet connection. Please note that you will be required to show your Toronto Metropolitan University OneCard prior to beginning to write the exam. In cases where you do not have a Toronto Metropolitan University OneCard, government issued ID is permitted.

Information will be provided prior to the exam date by your instructor who may provide an opportunity to test your set-up or provide additional information about online proctoring. Since videos of you and your environment will be recorded while writing the exam, please consider preparing the background (room / walls) so that personal details are not visible, or move to a room that you are comfortable showing on camera.

Academic Integrity

Toronto Metropolitan University's Policy 60 (the Academic Integrity policy) applies to all students at the University. Forms of academic misconduct include plagiarism, cheating, supplying false information to the University, and other acts. The most common form of academic misconduct is plagiarism - a serious academic offence, with potentially severe penalties and other consequences. It is expected, therefore, that all examinations and work submitted for evaluation and course credit will be the product of each student's individual effort (or an authorized group of students). Submitting the same work for credit to more than one course, without instructor approval, can also be considered a form of plagiarism.

Suspicions of academic misconduct may be referred to the Academic Integrity Office (AIO). Students who are found to have committed academic misconduct will have a Disciplinary Notation (DN) placed on their academic record (not on their transcript) and will normally be assigned one or more of the following penalties:

1. A grade reduction for the work, ranging up to an including a zero on the work (minimum penalty for graduate work is a zero on the work);
2. A grade reduction in the course greater than a zero on the work. (Note that this penalty can only be applied to course components worth 10% or less, and any additional penalty cannot exceed 10% of the final course grade. Students must be given prior notice that such a penalty will be assigned (e.g. in the course outline or on the assignment handout);
3. An F in the course;
4. More serious penalties up to and including expulsion from the University.

The unauthorized use of intellectual property of others, including your professor, for distribution, sale, or profit is expressly prohibited, in accordance with Policy 60 (Sections 2.8 and 2.10). Intellectual property includes, but is not limited to:

1. Slides
2. Lecture notes
3. Presentation materials used in and outside of class
4. Lab manuals
5. Course packs
6. Exams

For more detailed information on these issues, please refer to the Academic Integrity policy(https://www.torontomu.ca/senate/policies/pol60.pdf) and to the Academic Integrity Office website (https://www.torontomu.ca/academicintegrity).

Academic Accommodation Support

Toronto Metropolitan University acknowledges that students have diverse learning styles and a variety of academic needs. If you have a diagnosed disability that impacts your academic experience, connect with Academic Accommodation Support (AAS). Visit the AAS website or contact aasadmin@ryerson.ca for more information.

Note: All communication with AAS is voluntary and confidential, and will not appear on your transcript.

Important Resources Available at Toronto Metropolitan University

1. The Library provides research workshops and individual assistance. If the University is open, there is a Research Help desk on the second floor of the library, or students can use the Library's virtual research help service at https://library.torontomu.ca/ask to speak with a librarian.

2. Student Life and Learning Support offers group-based and individual help with writing, math, study skills, and transition support, as well as resources and checklists to support students as online learners.

3. You can submit an Academic Consideration Request when an extenuating circumstance has occurred that has significantly impacted your ability to fulfill an academic requirement. You may always visit the Senate website and select the blue radial button on the top right hand side entitled: Academic Consideration Request (ACR) to submit this request).

   Please note that the Provost/Vice President Academic and Deans approved a COVID-19 statement for Fall 2022 related to academic consideration. This statement will be built into the Online Academic Consideration System and will also be on the

Senate website (www.ryerson.ca/senate) in time for the Fall term:

Policy 167: Academic Consideration for Fall 2022 due to COVID-19: Students who miss an assessment due to cold or flu-like symptoms, or due to self-isolation, are required to provide a health certificate. All absences must follow Senate Policy 167: Academic Consideration.

Also NOTE: Policy 167: Academic Consideration does allow for a once per term academic consideration request without supporting documentation if the absence is less than 3 days in duration and is **not for a final exam/final assessment**. If the absence is more than 3 days in duration and/or is for a final exam/final assessment, documentation is required. For more information please see Senate Policy 167: Academic Consideration.

4. TMU COVID-19 Information and Updates for Students summarizes the variety of resources available to students during the pandemic.

5. TMU COVID-19 Vaccination Policy.

6. If taking a remote course, familiarize yourself with the tools you will need to use for remote learning. The Remote Learning guide for students includes guides to completing quizzes or exams in D2L Brightspace, with or without Respondus LockDown Browser and Monitor, using D2L Brightspace, joining online meetings or lectures, and collaborating with the Google Suite.

7. Information on Copyright for students.

8. At Toronto Metropolitan University (TMU), we recognize that things can come up throughout the term that may interfere with a student's ability to succeed in their coursework. These circumstances are outside of one's control and can have a serious impact on physical and mental well-being. Seeking help can be a challenge, especially in those times of crisis.

   If you are experiencing a mental health crisis, please call 911 and go to the nearest hospital emergency room. You can also access these outside resources at anytime:
   - **Distress Line:** 24/7 line for if you are in crisis, feeling suicidal or in need of emotional support (phone: 416-408-4357)
   - **Good2Talk:** 24/7 hour line for postsecondary students (phone: 1-866-925-5454)
   - **Keep.meSAFE:** 24/7 access to confidential support through counsellors via My SSP app or 1-844-451-9700

   If non-crisis support is needed, you can access these campus resources:

   - Centre for Student Development and Counselling: 416-979-5195 or email csdc@ryerson.ca
   - Consent Comes First - Office of Sexual Violence Support and Education: 416-919-5000 ext: 553596 or email osvse@ryerson.ca

   We encourage all Toronto Metropolitan University community members to access available resources to ensure support is reachable. You can find more resources available through the Toronto Metropolitan University Mental Health and Wellbeing website.