

## Course Outline (F2025)

### BME328: Digital Systems

<b>Instructor(s)</b>	Dr. Nagi Mekhiel [Coordinator] Office: ENG446 Phone: (416) 979-5000 x 557251 Email: nmekhiel@torontomu.ca Office Hours: Mon 2-3 PM, or Th 9-10 AM
<b>Calendar Description</b>	This course covers the basics digital logic circuits and emphasizes on good understanding of basic concepts in modern digital system design. The course introduces computer aided design (CAD) tools including the use of hardware description language (HDL) for design entry. It also discusses the use of the latest available implementation technologies including CPLDs and FPGAs for mapping the design to modern technology. This course covers basic logic circuits, Boolean algebra, and implementation technology (from transistor to CPLDs and FPGAs). It also introduces logic functions optimization and implementation, number representation and arithmetic circuits, combinational circuits, synchronous and asynchronous sequential circuits as well as introduction to control unit data path and CPU operations. The Laboratory work requires the uses of CAD tools to design and simulate basic digital circuits. Implementation and testing of simple digital systems in LSI and CPLD will also be considered.
<b>Prerequisites</b>	CPS 188, ELE 202, MTH 240
<b>Antirequisites</b>	None
<b>Corerequisites</b>	None
<b>Compulsory Text(s):</b>	<ol style="list-style-type: none"> <li>1. Brown, S. and Vranesic, Z. Fundamentals of Digital Logic with VHDL Design, Third Edition, McGraw-Hill, 2009. or 4th Edition 2023.</li> <li>2. Hayes, J. Introduction to Digital Logic Design, Addison Wesley, 1993. (Library call number TK7868.L6H29 1993).</li> <li>3. Laboratory Manual: Available through <a href="https://my.ryerson.ca/">https://my.ryerson.ca/</a> (D2L) or the course web page: <a href="http://www.ee.ryerson.ca/~courses/coe328">http://www.ee.ryerson.ca/~courses/coe328</a></li> </ol>
<b>Reference Text(s):</b>	<ol style="list-style-type: none"> <li>1. Wakerly, J. Digital Design: Principles and Practices, Prentice Hall, 2003. (Library call number TK7874.65.W34 2000).</li> <li>2. Dewey, A. Analysis and Design of Digital Systems with VHDL, PWS Publishing Company, 1997. (Library call number TK7868D5D47 1997).</li> </ol>
<b>Learning Objectives (Indicators)</b>	<p>At the end of this course, the successful student will be able to:</p> <ol style="list-style-type: none"> <li>1. Demonstrate an in-depth understanding of key concepts of digital systems and corresponding mathematical analysis tools. <b>(1c)</b></li> <li>2. Uses technical knowledge, design methodology, and appropriate design tools and related resources. Selects and uses an appropriate method for problem definition. <b>(4a)</b></li> <li>3. Describes differences between methods, performs a specified method in hypothetical design situation. <b>(4b)</b></li> </ol>

	<p>4. Develops further knowledge of using modern instrumentation, data collection techniques, and equipment to conduct experiments and obtain valid data. <b>(5a)</b></p> <p>5. Manages time effectively to achieve individual and team goals. <b>(6a)</b></p> <p>6. Reads and appropriately responds to technical and non-technical written instructions. <b>(7a)</b></p> <p>7. Understands the impact of his/her decisions and activities on the environment. <b>(9a)</b></p> <p><b>NOTE:</b>Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).</p>												
<b>Course Organization</b>	<p>4.0 hours of lecture per week for 13 weeks</p> <p>3.0 hours of lab per week for 12 weeks</p> <p>0.0 hours of tutorial per week for 12 weeks</p>												
<b>Teaching Assistants</b>	TBA												
<b>Course Evaluation</b>	<table border="1"> <thead> <tr> <th colspan="2">Theory</th></tr> </thead> <tbody> <tr> <td>Midterm Exam</td><td>30 %</td></tr> <tr> <td>Final Exam (40% theory 10% Labs)</td><td>40 %</td></tr> <tr> <th colspan="2">Laboratory</th></tr> <tr> <td>Lab Reports</td><td>30 %</td></tr> <tr> <td>TOTAL:</td><td>100 %</td></tr> </tbody> </table> <p><b>Note:</b> In order for a student to pass a course, a minimum overall course mark of 50% must be obtained. In addition, for courses that have both <b>"Theory and Laboratory"</b> components, the student must pass the Laboratory and Theory portions separately by achieving a minimum of 50% in the combined Laboratory components and 50% in the combined Theory components. Please refer to the <b>"Course Evaluation"</b> section above for details on the Theory and Laboratory components (if applicable).</p>	Theory		Midterm Exam	30 %	Final Exam (40% theory 10% Labs)	40 %	Laboratory		Lab Reports	30 %	TOTAL:	100 %
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<b>Examinations</b>	<p>Midterm exam in Week 7 or 8, two hours, closed book (covers Weeks 1-6).</p> <p>Final exam, during exam period, two and half hours, closed-book (covers Weeks 1-13).</p>												
<b>Other Evaluation Information</b>	None												
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## Course Content

Week	Hours	Chapters / Section	Topic, description
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1	1		INTRODUCTION TO BME328
1-2	4		INTRODUCTION TO LOGIC CIRCUITS (Chapter 2 Sections 2.1 to 2.10)
2-3	4		IMPLEMENTATION TECHNOLOGY (Chapter 3 Sections 3.1 to 3.10)
3-4	4		OPTIMIZATION OF COMBINATIONAL LOGIC (Chapter 4 Sections 4.2 to 4.12)
4-5	4		NUMBER REPRESENTATION AND ARITHMETIC CIRCUITS (Chapter 5 Sections 5.1 to 5.8)
5-6	4		COMBINATIONAL CIRCUIT BUILDING BLOCKS (Chapter 6 Sections 6.1 to 6.6)
6-8	8		INTRODUCTION TO SEQUENTIAL CIRCUITS (Chapter 7 Sections 7.1 to 7.13)
8-10	8		SYNCHRONOUS SEQUENTIAL CIRCUITS (Chapter 8 Sections 8.1 to 8.9)
10-11	4		ASYNCHRONOUS SEQUENTIAL CIRCUITS (Chapter 9 Sections 9.1 to 9.6)
11-12	4		REGISTER-LEVEL DESIGN (Hayes. pp. 599-605 609-611613)
12-13	6		SYSTEM ARCHITECTURE (Hayes 715-721)

## Laboratory(L)/Tutorials(T)/Activity(A) Schedule

Week	L/T/A	Description
2	TBA	Lab#1
2-3	TBA	LAB#1 (10 marks)
4	TBA	Functional Implementation &Minimization LAB#2 (10 marks)
5-6	TBA	Adder and Subtractor Unit LAB#3 and Lab#4 (15 Marks)
7	TBA	VHDL for Combinational Circuits and Storage Elements LAB#5 (15 marks)
8	TBA	Combinational Circuits and Storage Elements LAB#5 Continue
9-10	TBA	Sequential Circuits: Implementing an Eight State Machine LAB#6 (15 marks)
11-13	TBA	Simple Processor Module LAB#7 (35 marks)

## University Policies & Important Information

Students are reminded that they are required to adhere to all relevant university policies found in their online course shell in D2L and/or on [the Senate website](#)

Refer to the [Departmental FAQ page](#) for further information on common questions.

## Important Resources Available at Toronto Metropolitan University

- [The University Libraries](#) provide research [workshops](#) and individual consultation appointments. There is a drop-in Research Help desk on the second floor of the library, and students can use the [Library's virtual research help service](#) to speak with a librarian, or [book an appointment](#) to meet in person or online.
- [Student Life and Learning Support](#) offers group-based and individual help with writing, math, study skills, and transition support, as well as [resources and checklists to support students as online learners](#).
- You can submit an [Academic Consideration Request](#) when an extenuating circumstance has occurred that has significantly impacted your ability to fulfill an academic requirement. You may always visit the [Senate website](#) and select the blue radio button on the top right hand side entitled: Academic Consideration Request (ACR) to submit this request.

*For Extenuating Circumstances, [Policy 167: Academic Consideration](#) allows for a once per semester ACR request without supporting documentation if the absence is less than 3 days in duration and is not for a final exam/final assessment. Absences more than 3 days in duration and those that involve a final exam/final assessment, always require documentation. Students must notify their faculty/contract lecturer once a request for academic consideration is submitted. See Senate [Policy 167: Academic Consideration](#).*

Longer absences are not addressed through Policy 167 and should be discussed with your Chair/Director/Program to be advised on next steps.

- [FAQs Academic Considerations and Appeals](#)
- Information on Copyright for [Faculty/Contract Lecturers](#) and [students](#).

## Lab Safety (if applicable)

Students are to strictly adhere and follow:

- a. The Lab Safety information/guidelines posted in the respective labs,
- b. provided in their respective lab handouts, and
- c. instructions provided by the Teaching Assistants/Course instructors/Technical Staff.

During the lab sessions, to avoid tripping hazards, the area around the lab stations should not be surrounded by bags, backpacks etc, students should place their bags, backpacks etc against the walls of the labs and/or away from their lab stations in such a way that it avoids tripping hazards.

## Accessibility

- Similar to an [accessibility statement](#), use this section to describe your commitment to making this course accessible to students with disabilities. Improving the accessibility of your course helps minimize the need for accommodation.
- Outline any technologies used in this course and any known accessibility features or barriers (if applicable).
- Describe how a student should contact you if they discover an accessibility barrier with any course materials or technologies.

## Academic Accommodation Support

Academic Accommodation Support (AAS) is the university's disability services office. AAS works directly with incoming and returning students looking for help with their academic accommodations. AAS works with any student who requires academic accommodation regardless of program or course load.

- Learn more about [Academic Accommodation Support](#).
- Learn [how to register with AAS](#).
- Learn about [Policy 159: Academic Accommodation of Students with Disabilities](#)

Academic Accommodations (for students with disabilities) and Academic Consideration (for students faced with extenuating circumstances that can include short-term health issues) are governed by two different university policies. Learn more about [Academic Accommodations versus Academic Consideration and how to access each](#).

## Wellbeing Support

At Toronto Metropolitan University, we recognize that things can come up throughout the term that may interfere with a student's ability to succeed in their coursework. These circumstances are outside of one's control and can have a serious impact on physical and mental well-being. Seeking help can be a challenge, especially in those times of crisis.

If you are experiencing a mental health crisis, please call 911 and go to the nearest hospital emergency room. You can also access these outside resources at anytime:

- **Distress Line:** 24/7 line for if you are in crisis, feeling suicidal or in need of emotional support (phone: 416-408-4357)

- **Good2Talk**: 24/7-hour line for postsecondary students (phone: 1-866-925-5454)
- **Keep.meSAFE**: 24/7 access to confidential support through counsellors via [My SSP app](#) or 1-844-451-9700

If non-crisis support is needed, you can access these campus resources:

- **Centre for Student Development and Counselling**: 416-979-5195 or email [csdc@torontomu.ca](mailto:csdc@torontomu.ca)
- **Consent Comes First - Office of Sexual Violence Support and Education**: 416-919-5000 ext 3596 or email [osvse@torontomu.ca](mailto:osvse@torontomu.ca)
- **Medical Centre**: call (416) 979-5070 to book an appointment

We encourage all Toronto Metropolitan University community members to access available resources to ensure support is reachable. You can find more resources available through the [Toronto Metropolitan University Mental Health and Wellbeing](#) website.