CURRICULUM VITA - Gul N. Khan

Formal Qualifications: B.Sc., B.Eng., M.Sc., DIC, Ph.D., P.Eng., SMIEEE

Office and Mailing Address: Department of Electrical and Computer Engineering,
Ryerson University, 350 Victoria Street,
Toronto, Ontario M5B 2K3, Canada
Tel: (Off) (416) 979-5000 ext.556084 Facsimile: (416) 979-5280
Email: gnkhan@ryerson.ca URL: http://www.ee.ryerson.ca/~gnkhan
https://www.torontomu.ca/electrical-computer-biomedical/people/faculty/gul-khan/

Teaching and Research Interests

Heterogeneous Computing, Network on Chip, MPSoC, CPU-GPU Systems, Embedded Systems on a Chip, Hardware Software Codesign, Fault-Tolerant Software Systems, System Partitioning, Distributed Systems and Computer Networks, High Performance Computer Systems, Machine Vision and Intelligent Systems.

Education

- ***Ph.D.*** in Computing — July 1989
  Imperial College of Science Technology and Medicine, University of London.
- ***M.Sc.*** in Computer Engineering — August 1982
  Syracuse University, Syracuse New York.
- ***B.Sc.*** in Electrical Engineering — February 1979
  University of Engineering and Technology, Lahore Pakistan.
- ***B.Sc.*** in Maths and Physics — December 1973
  Government College, Lahore. (Punjab University, Lahore Pakistan)

Experience Summary

• *Professor, Computer Engineering*	Ryerson University, Toronto, Canada	2016 - Present
• *Professor, Program Director for Computer Engineering*	Ryerson University, Toronto, Canada	2012- 2016
• *Associate Professor, Program Director for Computer Engineering*	Ryerson University, Toronto, Canada	2004- 2012
• *Associate Professor*	Ryerson University, Toronto, Canada	2001- 2004
• *Associate Professor*	University of Saskatchewan, Canada	2000- 2001
• *Affiliate Professor*	TRLabs, Saskatoon Saskatchewan Canada	2000- 2001
• *Associate Professor*	Nanyang Technological University, Singapore	1997 - 2000
• *Associate Professor and Head of Computer Engineering Department*	EME College, National University of Science & Technology Pakistan	1995 - 1997
• *Principal Engineer*	Institute of Industrial Automation (KRL), Pakistan	1989 - 1995
• *Visiting Researcher*	RMIT University Melbourne Australia	1993 - 1994
• *Visiting Professor*	Quaid-i-Azam University, Islamabad Pakistan	1989-93, 1994-95
• *Research Assistant*	Imperial College, University of London, UK	1986 - 1989
• *Senior Engineer*	Institute of Industrial Automation (KRL), Pakistan	1983 - 1986
• *Research Associate*	Arizona State University, AZ, USA	1982 - 1983
• *Research Assistant*	Syracuse University, NY, USA	1982 - 1982
• *Consulting Design Engineer*	WAPDA Pakistan	1979 - 1981

Courses Taught

- Data Structures, Embedded Software Systems, Operating Systems, Real-time Systems, Software Engineering;
- Systems-on-Chip Design, Computer Vision, Digital Image Processing, Robot and Autonomous Navigation;
- Parallel Processing Architecture, Distributed Processing, Data Communication, Wide Area Networks;
- Digital Systems & Logic Design, Computer Organization and Architecture, Embedded Computer Systems, Digital Electronics, Circuit Elements in Digital Computation, Microprocessor Systems, System on Chip Design.

Substantial Research Projects Completed or in progress

Project Title	*Role and Contribution*	*Project Duration & Sponsoring Agency*	*Outcome of the Project*
• Automatic Endoscope	Founding Member	1987-1992 Olympus Optical Co. Tokyo, Japan	Prototype automatic colonoscope developed. 3 US patents accepted.
• KSM: A Parallel Super Microcomputer	Project Leader	1989-1993 Institute of Industrial Automation, Pakistan	Developed 256 -1024 node parallel computer systems.
• Development of Parallel System for Signal Processing	Co-investigator	1991-1993 NSRDB, Pakistan	Implemented TMS320 DSP and T800 series transputer based parallel system
• Image transmission via low bandwidth wireless channels in hostile environment.	Project Leader	1995-1997 E&ME College/Core Pak. Army Rawalpindi	Developed fault-tolerant image compression algorithms and prototype image receiver/transmitter
• Content based image retrieval system for trademark logo's	Principal Investigator	2000-2001 Univ. of Saskatchewan ($17,000)	Image feature extraction for indexing and searching of trademark database
• Embedded System for Endoscope Navigation	Principal Investigator	2000-2005 NSERC DG, Canada ($105,000)	Hardware-Software code sign of high performance & fault-tolerant embedded system
• CAD tools for co-synthesis of embedded systems for smart home control	Principal Investigator	2006-2009 NSERC DG, Canada ($54,000)	Smart home embedded systems synthesized to be used for the elderly and handicapped
• Multi-core embedded systems: computer aided NOC/MPSOC design & simulation.	Principal Investigator	2010-2016 NSERC DG, Canada ($140,000)	NoC design and synthesis tools
• CAD Tools for Multi/Many-core NoC and Heterogeneous Computing System Design.	Principal Investigator	2018-2019 NSERC DG, Canada ($23,000)	Design Tools for Heterogeneous CPU-GPU and NoC Systems

Awards and Honours

2000-2019: Discovery Grants Individual, NSERC Canada.
1997-98: Honorary Chairman IEEE (Pak. Sec.) Awards and Conferences
1993-94: Senior Research Fellow, RMIT University, Melbourne Australia.
1986-89: Imperial College Bursary, University of London UK.
1987-89: Overseas Research Student Award, CVCP, UK.
1981-82, 1986-89: Quaid-i-Azam Scholarship, Ministry of Education, Pakistan.
1982-83: Board of Regents Scholarship, Arizona State University, Tempe Arizona USA.
1979: University Gold Medal and Ranked First in University of Engineering and Technology, Lahore Pakistan.
1974-78: Merit Scholarship, BEng Electrical Engineering, UET, Lahore Pakistan.
1973: Merit Scholarship and Ranked First in Government College, Lahore Pakistan.
1969: Merit Scholarship and Ranked First in Secondary School

Academic Experience

- July 2001- Present

Professor – Computer Engineering (Sept. 2015-Present)
Professor and Program Director for Computer Engineering (2004-Sept. 2015)
Department of Electrical and Computer Engineering, Ryerson University, Toronto Canada.
Teaching under-graduate subjects in the areas of embedded software systems, real-time systems, hardware-software codesign of embedded systems, computer architecture, wide area networks and operating systems. Supervising R&D projects in the areas of embedded and real-time systems, hardware software codesign, co-synthesis and system partitioning.
Responsible for the academic management of computer engineering program. Main research and industrial projects being investigated include:

1. Network-on-Chip and Multiprocessor Systems-on-Chip design and simulation techniques.
2. RFID smart systems and authentication protocols.
3. Hardware-software system partitioning techniques for embedded system and system-on-chip design.
4. Safety critical high performance embedded system development intended for multimedia and medical applications including endoscope navigation.
5. Fault-tolerant real-time scheduling techniques.
6. Fault-tolerant message passing and multicasting systems.
7. Smart home embedded systems.

- July 2000 - June 2001

Associate Professor of Computer Engineering
Department of Electrical Engineering, University of Saskatchewan, Saskatoon Canada.
Taught undergraduate courses in the areas of digital circuits, digital system synthesis and microprocessor systems. Supervised research projects in the areas of intelligent systems and fault-tolerant embedded computer systems. Main research and industrial projects included: hardware software co-design of embedded computer systems for critical control and content-based image retrieval systems.

- June 1997 - June 2000

Associate Professor
School of Computer Engineering, Nanyang Technological University, Singapore.
Taught under graduate subjects in the areas of computer architecture, digital system synthesis using VHDL and microprocessor systems. Supervised R&D projects in the areas of fault-tolerant software systems, computer vision, multimedia systems and embedded systems. Main research and industrial projects include:

1. Safety critical high performance embedded systems for control applications.
2. Hardware software co-design of embedded systems.
3. Content-based image retrieval and database management of trademark logos.
4. Development of FPGA based low cost micro-controllers.
5. Distributed recovery block approach-based fault-tolerant message passing and multicasting.

- October 1995 - June 1997

Associate Professor and Head Department of Computer Engineering.
College of E & ME, National University of Sciences and Technology, Islamabad Pakistan.
Led the team that developed curriculum, teaching and research facilities for under-graduate and graduate programs being offered in computer engineering. Taught under graduate and postgraduate courses in the areas of parallel and distributed processing, computer vision, digital image processing and computer architectures. Supervised research projects related to computer vision, fault-tolerant computing and multimedia. Main projects include:

1. Image transmission on wireless channels in hostile and noisy environments.
2. Fault-tolerant radar tracking algorithms.
3. Error-tolerant image compression techniques.

- July 1993 - July 1994

Visiting Professor
Computer Systems Engineering, RMIT University, Melbourne Australia.
Taught under-graduate and graduate courses including computer vision, image processing, parallel processing systems and advance computer architectures. Conducted research on real-time and fault-tolerant machine vision techniques for industrial automation at High Performance Computer Centre, RMIT University.

- September 1989 - June 1993 and July 1994 - July 1995

Visiting Professor
Department of Electronics, Quaid-i-Azam University, Islamabad Pakistan.
Taught graduate courses including computer vision, digital image processing, advance computer systems, distributed processing and software engineering. Participated in the feasibility study and development of a DSP based high-performance computer system. This project was funded by NSRDB.

- January 1981- August 1982

Research Assistant
Electrical and Computer Engineering, Syracuse University, Syracuse New York USA

Industrial Experience

- August 1989 - June 1993 and July 1994 - October 1995

Principal Engineer (12/90 -10/95), Headed the Supercomputing and Distributed Processing Group.
Institute of Industrial Automation (KRL), Islamabad Pakistan.
Following are the sample research and development projects undertook and completed successfully by Supercomputing and Distributed Processing Group:

1. Embedded computer control system design and development for chemical and nuclear centrifuge enrichment plants.
2. Development of software and hardware for microprocessor-based industrial control and monitoring.
3. Development of algorithms for machine vision, autonomous navigation and multimedia data processing.
4. Led the team of researchers and engineers to develop TDRP-series high performance parallel computer systems and their support software including message passing, distributed operating systems and bench marking.
5. Investigation, design and development of re-configurable MIMD computer systems to achieve high performance computing.
6. Provided consultation for software engineering related distributed computing projects for hospital management and library automation.

- July 1993 - July 1994

Visiting Senior Research Fellow
Centre for Advancement in Information Technology (CITRI) RMIT, Melbourne Australia.
Conducted research on real-time and fault-tolerant machine vision techniques for industrial automation at the High-Performance Computer Centre at CITRI RMIT University.

- October 1986 - July 1989

Research Assistant
Department of Computing, Imperial College of Science, Technology and Medicine

University of London, 180 Queens Gate, London SW7 2BZ England.

1. Conducted research and development work in the areas of machine vision, biomedical engineering, parallel processing and autonomous navigation.
2. This research at Imperial College was funded by Olympus Optical Co. Tokyo and resulted in three successful US patents.

- June 1983 - September 1986

Senior Engineer, Headed the Micro-computer System Section
Institute of Industrial Automation (KRL), Islamabad Pakistan.
Designed and developed microprocessor-based embedded industrial control and monitoring software and hardware systems.

- September 1982 - May 1983

Research Associate
Electrical and Computer Engineering, Arizona State University, Tempe, Arizona 85287 USA
Developed a variety of speech and image processing techniques.

- March 1979 - April 1981

Consulting Design Engineer, Water and Power Development Authority, Lahore Pakistan.
Designed and provided consultation for protection and control systems of 132/220kv grid stations.

Professional and Academic Activities

- Topic Editor: Micromachines, MDPI
- Guest Editor: Micromachines, Special Issue "Network-on-Chip and Application"
- Associate Editor: Int. J. Embedded and Real-time Communication System (IGI Global)
- Associate Editor: Int. Journal of Reconfigurable and Embedded Systems
- Senior Member IEEE
- Professional Engineer, PEO Ontario, Canada
- Member, Advisory Committee for B.Sc. in Software Systems and Humber College Toronto, 2002-03
- Chair Department Council, Electrical & Computer Engineering (Ryerson University), 2002-present
- Program Director Computer Engineering Ryerson University 2004-2015
- Member, Graduate Program Committee Ryerson University, 2002-2005
- Examiner PEO (Professional Engineers Ontario) National Exam Digital Logic Circuits, 2002-Present
- Chairman IEEE (Pak. Sec.) Awards and Conference Committee, 1997

Member Organizing Committee and/or Technical Program Organizer

- 7th Int. workshop Engineering Parallel and Multi-Core Systems, 2014, 2015, 2016, 2017, 2018.
- Int. Conf. on Pervasive and Embedded Computing and Communication Systems, Lisbon 2014
- PC Chair, Int. Wks Engineering Parallel and Multi-Core Systems, Taiwan July 2013
- Int. Symp. Embedded Multi-Core Systems-on-Chip 2007 to 2012, 2015-2021.
- Int. Conf. Image Analysis and Recognition, 2005 to 2011.
- IEEE/IFIP Conf. Embedded and Ubiquitous Computing Vancouver, August 2009
- IEEE Pak. 2nd Multi Topic Conference, GIK Institute Topi, Pakistan, 1995, 1997.
- Int. Workshop on Computer Vision & Parallel Processing, Islamabad Pakistan, January 1995.
- National Workshop on Parallel Computing: Architecture's and Applications, Department of Electronics, Quaid-i-Azam University Islamabad, Pakistan, 26-30 April 1992.

Member Technical Program Committee and/or Session Chair

- IEEE Asia Pacific Conference on Circuits and Systems (APCCAS'21) Penang, Malaysia November 22-26, 2021
- IEEE Nordic Circuits and Systems Conference, (NorCAS) Oslo Norway, October 26-27, 2021
- IEEE Nordic Circuits and Systems Conference, (NorCAS) Virtual, October 27-28, 2020
- IADIAS 16th Int. Conf. on Applied Computing (AC2019) 2019.
- IEEE Int. Symp. on Embedded Multi/Many Core Systems-on-Chip (MCSoC), 2010, 2015–2021.

- IEEE Annual Conf. Ubiquitous Computing, Electronics and Mobile Communication (IEEE UEMCON) 2016, 2017, 2018.
- Int. Workshop Security, Privacy and Trustworthiness in Medical Cyber Physical System (Chase 2016) Washington, June 2016.
- Int'l Conf. on Pervasive and Embedded Computing and Communication Systems, PECSS 2013-2020.
- IEEE Int. Conf. on Computer Communications and Networks Workshops (MobiPST), 2011-2016.
- IEEE 8th Int. Conf. Complex, Intelligent and Software Intensive Systems Workshops. 2014-2018.
- IEEE Canadian Conference on Electrical and Computer Engineering, 2002, 2004, 2008, 2011, 2013
- 20th IEEE Int. Conf. on Computer Communications and Networks Workshops (ETMEC: Energy & Thermal Management of Embedded Computing), Maui, July- Aug 2011.
- 39th International Conference on Parallel Processing, San Diego, September 2010.
- Int. Conf on Image Analysis and Recognition 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2011.
- International Conferences for Upcoming Engineers, Toronto, May 2003, 2004.

Reviewer

- Microprocessors and Microsystems Journal
- Journal of Software and Systems.
- IEEE Transaction on Computers.
- Int. Journal Design Automation for Embedded Systems.
- IEEE Canadian Conference on Electrical and Computer Engineering, May 2004 to 2013.
- Int. Conf. on Parallel and Distributed Systems (PDCS) 2002.
- Int. Conf. on Embedded Systems and Applications, ESA'03, 2003
- NSERC Discovery, CHRP and Strategic grant applications.

Invited Speaker

- CMOS ET, Whistler BC Canada 2010.
- Careers in Computer Engineering Industry, Career 2000 Seminar & Exhibition Singapore, 9-12 Mar 2000.
- Int. Workshop on Computer Vision and Parallel Processing, Islamabad, Pakistan, 2-5 January 1995.
- International Workshop on Pattern Recognition, Image Understanding and Artificial Neural Networks, Shanghai Jiao Tong University, Shanghai China, 28-30 September 1992.
- National Workshop on Parallel Computing: Architecture's and Applications, Department of Electronics, Quaid-i-Azam University Islamabad, Pakistan, 26-30 April 1992.

Publications

Refereed Journal Papers, Book Chapters and Patents

1. D. Lee, F. Yuan, **Gul N. Khan** and Y. Zhou "A 8-bit digital-to-time converter with pre-skewing and time interpolation," *IET Circuits, Devices & Systems.* Vol. 15, No. 7, pp. 670-685, October 2021.
2. Masoud Oveis-Gharan, **Gul N. Khan** "Reconfigurable on-chip interconnection networks for high performance embedded SoC design" *Journal of System Architecture*, Vol. 106, pp. 1-17, June 2020.
3. Mohid Tayyub and **Gul N. Khan** "Heterogeneous Design and Efficient CPU-GPU Implementation of Collision Detection", IADIS International Journal on Computer Science and Information Systems, Vol. 14, No. 2, pp. 25-40, July-Dec. 2019.
4. **Gul N. Khan**, "Efficient and Low Power NoC Router Architecture" in High-Speed and Low Power Technologies: Electronics and Photonics, Eds. Jung Choi and Kris Iniewski (CRC Press) Taylor & Francis, pp. 211-251, 2018.
5. M. Obaidullah and **Gul N. Khan** "Application Mapping to Mesh NoCs using a Tabu-Search based Swarm Optimization" *Microprocessors and Microsystems*, Vol. 55, pp. 13-25, November 2017.
6. Fei Yuan and **Gul Khan** "All-Digital Gated Ring Oscillator ΔΣ Modulators "*Journal Analog Integrated Circuits and Signal Processing*, Vol. 92, Issue 7, pp. 483-488, September 2017.
7. Masoud Oveis-Gharan and **Gul N. Khan** "Efficient Dynamic Virtual Channel Organization and Architecture for NoC Systems" *IEEE Transactions VLSI Systems*, Vol. 24 No.2, pp. 465-478, Feb. 2016.

8. **Gul N. Khan** and Markus Moessner "Low-cost authentication protocol for passive, computation capable RFID tags" *Wireless Networks, Journal of Mobile Communication, Computation and Information,* Vol. 21, No. 2, pp. 565-580, February 2015.
9. Masoud Oveis-Gharan and **Gul N. Khan** "Statically Adaptive Multi-FIFO Buffer Architecture for Network-on-Chip" *Microprocessors and Microsystems*, Vol. 39, No. 1, pp. 11-26, February 2015.
10. Masoud Oveis-Gharan and **Gul N. Khan** "Packet-based Adaptive Virtual Channel Configuration for NoC Systems" *Int. Journal of Computation and Digital Systems*, Vol. 4, No. 1, pp. 5-18, January 2015.
11. **Gul N. Khan**, "Co-synthesis of Real-time Embedded Systems" in ***Embedded and Networking Systems: Design, Software and Implementation,*** *Eds. Gul Khan and Kris Iniewski, (*CRC Press) Taylor & Francis, pp. 21-55, 2014.
12. Anita Tino and **Gul N. Khan** "High Performance NoC Synthesis using Analytical Modelling and Simulation with Optimal Power and Minimal IC Area" *Journal of Systems Architecture*, Vol. 59, No. 7, pp. 1348-1363, November 2013.
13. G. Zhu, F. Yuan and **G. Khan** "Time-Mode Approach for Mixed Analog-Digital Signal Processing" *Journal of Electrical and Electronic Systems*, Vol. 2, No. 1, e109 pp. 1-4, January 2013.
14. Omesh Mutukuda, Andy Ye and **Gul Khan** "Utilizing Multi-Bit Connections to Improve the Area Efficiency of Unidirectional Routing Resources for Routing Multi-Bit Signals on FPGAs" *Microprocessors and Microsystems Journal,* Vol. 36, No.3, pp. 167-175, May 2012.
15. Markus Moessner and **Gul N. Khan** "Secure Authentication Scheme for Passive C1G2 RFID Tags" *Computer Networks Journal,* Vol. 56, No. 1, pp. 273-286, January 2012.
16. Anita Tino and **Gul N. Khan** "Designing Power and Performance Optimal Application Specific Network-on-Chip Architecture" *Microprocessors and Microsystems*, Vol. 35, No. 6, pp. 523-534, August 2011.
17. **Gul N. Khan** and V. Dumitriu, "A Modelling Tool for Simulating and Design of On-Chip Network Systems" *Microprocessors and Microsystems*, Vol. 34, No. 3-4, pp. 84-95, March-June 2010.
18. Y. Chen, F. Yuan and **Gul Khan**, "A Wide Dynamic Range CMOS PFM Digital Pixel Sensor with in-Pixel Variable Reference Voltage" *Int. Journal Analog Integrated Circuits and Signal Processing*, Vol. 61, No. 3, pp. 287-299, December 2009.
19. V. Dumitriu and **Gul N. Khan**, "Throughput Oriented NoC Topology Generation and Analysis for High Performance SoCs" *IEEE Transactions VLSI Systems*, Vol. 17, No. 10, pp. 1433-1446, October 2009.
20. Yong Chen, Fei Yuan and **Gul Khan**, "A Wide Dynamic Range CMOS Image Sensor with Pulse-Frequency-Modulation and in-Pixel Amplification" *Microelectronics Journal*, Vol. 40, No. 10, pp. 1496-1501, October 2009.
21. **Gul N. Khan** and U. Ahmed, "CAD Tool for Hardware Software Co-synthesis of Heterogeneous Multiple Processor Embedded Architectures" *Int. Journal Design Automation for Embedded Systems*, Vol. 12, No. 4, pp. 313-343, December 2008.
22. **Gul N. Khan,** "Smart Homes for the Disabled and Elderly" *Impact,* Vol. 4, No. 2, October 2006.
23. Y. H. Yang, A. A. Guergachi and **G. N. Khan**, "Support Vector Machines for Environmental Informatics: Application to Modelling the Nitrogen Removal Processes in Wastewater Treatment Systems" *Journal of Environmental Informatics,* Vol 7, No.1. pp. 14-25 March 2006.
24. Y. H. Yang, A. A. Guergachi and **G. N. Khan**, "Short Term Prediction in Nitrogen Removal Processes Using Least Squares Support Vector Machine with NARX Model" *Environmental Informatics Archives*, Vol 2, pp. 598-609, ISEIS Publication, 2004.
25. **Gul N. Khan** and Gu Wei, "Fault-tolerant Wormhole Routing using a Variation of Distributed Recovery Block Approach" *IEE Proceedings Computers and Digital Techniques,* Vol. 147, No. 6, pp. 397-402, November 2000.
26. Gu Wei and **Gul N. Khan**, "Using Distributed Recovery Block for Fault-tolerant Routing" *SAS Research Link*, Vol. 6/2000, Singapore, pp. 8-9, January 2000.
27. **Gul N. Khan**, "Fault-tolerance Evaluation of a High Performance Embedded Computer System" *SAS Research Link*, Vol. 5/99, Singapore, pp. 4-5, January 1999.
28. **Gul N. Khan**, "A Fault-tolerant Multiprocessor Architecture for High Performance Embedded Applications" *SAS Research Link*, Vol. 4/98, Singapore, pp. 9-10, January 1998.
29. **Gul N. Khan** and Duncan F. Gillies, "A Vision based Navigation System for an Endoscope" *Image and Vision Computing*, Vol. 14, No. 10, pp. 763-772, December 1996.

30. **Gul N. Khan**, K. Mahmud, M. S. Iqbal and H. U. Rashid, "RSM - A Restricted Shared Memory Architecture for High Speed Inter-processor Communication" *Microprocessors and Microsystems Journal*, Vol. 18, No. 4, pp. 193-203, May 1994.
31. **Gul N. Khan** and K. Mahmud, "A Scalable and Fault Tolerant Restricted Shared Memory Architecture" *Electronics Letters*, Vol. 29, No 9, pp. 783-785, April 1993.
32. **Gul N. Khan** and D. F. Gillies, "Parallel-Hierarchical Image Partitioning and Region Extraction" *Computer Vision and Image Processing*, Eds. L. Shapiro and A. Rosenfeld, pp. 123-140, Academic Press 1992.
33. **Gul N. Khan** and D. F. Gillies, "Extracting Contours by Perceptual Grouping" *Image and Vision Computing*, Vol. 10, No. 2, pp. 77-88, March 1992.
34. Duncan F. Gillies, **Gul N. Khan** and Y. Takahashi, "Methods of Detecting Endoscope Insertion Direction" US. Patent Number 5,036,464 July 30, 1991.
35. Duncan F. Gillies and **Gul N. Khan**, "Endoscope Insertion Direction Detecting Method" US. Patent Number 4,916,533 April 10, 1990.
36. Duncan F. Gillies and **Gul N. Khan**, "Endoscope Insertion Direction Detecting Method" US. Patent Number 4,910,590 March 20, 1990.
37. **Gul N. Khan** and D. F. Gillies, (Book Chapter) "A Highly Parallel Shaded Image Segmentation Method" in *Parallel Processing for Computer Vision and Display,* (Eds. P. Dew, R. Earnshaw and T. Heywood) pp. 180-189, Addison Wesley England, 1989.

Books and Proceedings Edited

Embedded and Networking Systems: Design, Software and Implementation, *Eds. Gul Khan and Kris Iniewski, (*CRC Press) Taylor & Francis, 2014

Gul N. Khan, M. A. Maud, A. Hussain (Eds.) Proceedings *IEEE 1st Multi-topic Conference*, EME College, Rawalpindi, 28-29 Nov. 1995.

Gul N. Khan, A. A. Naqvi and M. Shah (Eds.) Proceedings *Int. Workshop on Computer Vision and Parallel Processing*, Islamabad, 2-5 January 1995.

Gul N. Khan and A. A. Naqvi (Eds.) Proceedings *National Workshop on Parallel Computing: Architecture's and Applications*, Department of Electronics, Quaid-i-Azam University Islamabad, 26-30 April 1992.

Refereed Publications at Conferences, Workshops and Symposiums

1. Sunbal Cheema and **Gul N. Khan** "GPU Auto-tuning Framework for Optimal Performance and Power Consumption", *ACM Conf. Principles and Practice of Parallel Programming - ACM Wks General Purpose Processing using GPU (GPGPU 2023)* Feb. 24-March 1st, 2023, Montreal, Canada
2. Sunbal Cheema and **Gul N. Khan** "Power and Performance Analysis of Deep Neural Networks for Energy-aware Heterogeneous Systems", *IEEE Int. Conf. Systems, Man and Cybernetics* (SMC-20), Toronto, pp. 2184-2189, October 11-14, 2020.
3. Mohid Tayyub and **Gul N. Khan** "Heterogeneous CPU-GPU Implementation of Collision Detection", Proc. *16th International Conference on Applied Computing*, Cagliari Italy, pp. 71-78, November 7-9, 2019.
4. Daniel J. Lee, Fei Yuan and **Gul Khan** "Digitally Interpolated Pre-Skewed Delay-Line Digital-to-Time Converter with Minimum Nonlinearity and Latency", Proc. *IEEE 62nd International Midwest Symposium on Circuits & Systems*, Dallas, Texas USA August 4-7, 2019.
5. Abdullah Siddiqui and **Gul N. Khan** "Design Space Exploration of Embedded Applications on Heterogeneous CPU-GPU Platforms", Proc. *Int. Conf. High Performance Computing and Simulation (HPCS-19)*, Dublin, Ireland, July 15-19, 2019.
6. **Gul N. Khan** and Masood Oveis-Gharan "Application Specific Reconfigurable SoC Interconnection Network Architecture", Proc. *32nd International Conference on Architecture of Computing Systems* (Springer LNCS 11479, ARCS 2019) Copenhagen, Denmark, pp. 322-333, May 20-23, 2019.
7. Daniel J. Lee, Fei Yuan and **Gul Khan** "Architectures and Design Techniques of Digital Time Interpolators" *IEEE Proceedings 3rd Int. Conf. Integrated Circuits and Microsystems (ICICM 2018),* Shanghai China, pp. 15-20, November 24-26, 2018.
8. M. Obaidullah, F. Yuan and **Gul N. Khan** "Hybrid Multi-swarm Optimization based NoC Configuration and Synthesis" *Proceedings IEEE Nordic Circuits and Systems Conference (NORCAS 2018),* Tallinn, Estonia, pp. 1-6, October 30-31, 2018.

9. M. Oveis-Gharan and **Gul N. Khan** "Flexible Reconfigurable on-chip Networks for Multi-core SoCs" *ACM Proceedings 9th Int. Symp. on Highly-Efficient Accelerators and Reconfigurable Technologies (HEART 2018)*, Toronto, Canada, pp. 19:1-19:6, June 20-22, 2018.
10. M. Obaidullah and **Gul N. Khan** "Hybrid Multi-swarm Optimization Based NoC Synthesis" Proc. *30th IEEE Int. System-on-Chip Conf. (SOCC 2017),* Munich, Germany, pp. 62-67, September 5-8, 2017.
11. **Gul N. Khan** and Stephen Chui "Congestion Aware Routing for On-Chip Communication in NoC Systems" in Proc. *11th Int. Conf. Complex, Intelligent and Software Intensive Systems (ePaMuS'17),* Torino Italy, pp. 547-556, July 2017 (Springer Book Series Advances in Intelligent Systems and Computing 611, 2018).
12. M. Obaidullah and **Gul N. Khan** "Optimal Application Mapping to 2D-Mesh NoCs by using a Tabu-based Particle Swarm Methodology" in Proc. *2nd Int. Workshop Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (HiPEAC'17 Wks. AISTECS),* Stockholm Sweden, pp. 17-22, January 25, 2017.
13. M. O. Gharan and **Gul N. Khan** "Adaptive VC Organization and Arbitration for Efficient NoC Design" Proc. *IEEE Int. Symp. on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-16)*, Lyon, France, pp. 31-38, Sept. 21-23, 2016
14. Masoud O. Gharan and **Gul N. Khan "**Dynamic Virtual Channel and Index-based Arbitration based Network on Chip Router Architecture**"**, Proc. *IEEE Int. Conf. High Performance Computing and Simulation (HPCS-16)*, Innsbruck, Austria, pp. 96-103, July 18-22, 2016.
15. G. Zhu, F. Yuan, **Gul Khan "**A 0.13µm CMOS 5-MHz BW 47-dB SNDR All-Digital Time-Mode First Order Delta-Sigma ADC with 3-bit Gated VCO Quantizer**"**, Proc. *9th IEEE Int. Conf. on Electrical and Electronics Engineering,* Bursa, Turkey, pp. 29-32, November 26-28, 2015.
16. Masoud O. Gharan and **Gul N. Khan "**Dynamic VC Organization for Efficient NoC Communication**"**, Proc. *IEEE 9th Int. Symposium Embedded Multicore/Many-core Systems on Chip (MCSoC-15)*, Turin, Italy, pp. 151-158, Sept. 23-25, 2015.
17. Masoud O. Gharan and **Gul N. Khan "**Index-based Round-Robin Arbiter for NoC Routers**"**, Proc. *IEEE Computer Society Annual Symposium on VLSI*, pp. 62-67, Montpellier France July 8-10, 2015.
18. Masoud O. Gharan and **Gul N. Khan "**Efficient Virtual Channel Organization and Congestion Avoidance in Multicore NoC Systems**"**, Proc. *IEEE 26th Int. Symp Computer Architecture and High Performance Computing Wks (WAMCA'14)*, UPM Paris, pp. 30-35, October 2014.
19. Masoud O. Gharan and **Gul N. Khan** "Packet-based Adaptive Virtual Channel Configuration for NoC Systems", in Proc. *9th Int. Conf. on Future Networks and Communications* (DPNoC 2014) Procedia Computer Science Vol. 34, pp. 552–558, Niagara Falls, August 2014.
20. Masoud O. Gharan and **Gul N. Khan** "Dynamic Virtual Channel Configuration for Efficient Multicore Systems", Proc. *IEEE 8th Int. Conf. Complex, Intelligent and Software Intensive Systems Wks. (ePaMuS'14)* pp. 445-450*,* Birmingham, July 2-4, 2014.
21. Mohamed J. Hakeem, Kaamran Raahemifar and **Gul N. Khan** "Novel modulo based Aloha anti-collision algorithm for RFID systems", Proc. *IEEE Int. Conf. RFID*, pp. 97-102, Orlando FL, April 8-10, 2014.
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