EE8205: Embedded Computer Systems

Final Examination

General Instructions **Maximum Marks: 75**

a) Total time allowed is **2 hours**.
b) The examination has 5 pages and 5 questions. Answer all the questions.
c) To earn maximum credit, your answer must be concise and to the point.
d) Some questions contain special instructions. Please ensure that you read them carefully.
e) All questions are not of the same difficulty and value. Consider this when allocating time for their solution.
f) Estimated time for each question is equivalent to the marks assigned to it.
g) List all the assumptions you made for a particular solution.

1. a) Identify three advantages or uses of the interrupt facility provided in processors. ***MARKS: 5***

i)

ii)

iii)

b) List two schemes that are normally used to handle multiple interrupts. Which scheme is suitable to handle two interrupts one from a printer and the other from a LAN interface card?

MARKS: 5

2. Indicate (in the space provided) whether the following are TRUE or FALSE. To obtain full marks for each question, include a ***SHORT*** comment in support of your answer.

MARKS: 16 (2 each)

a) DMA-based I/O improves the efficiency of a computer system.
TRUE ___ or FALSE ___?

b) Blocking message-send and blocking message-receive is used for process synchronization.
TRUE ___ or FALSE ___?

c) Thread switching is more expensive as compared to process switching.
TRUE ___ or FALSE ___?

d) Context switching is related to system call.
TRUE ___ or FALSE ___?

e) When a process waits for an I/O event, it is moved from running state to ready state.
TRUE ___ or FALSE ___?

f) A cache hit means that the required information (Data/Code) is found in the main memory.
TRUE ___ or FALSE ___?

g) Processes with two priority levels will never lead to unbounded priority inversion.
TRUE ___ or FALSE ___?

h) The deadlines for hard real-time processes can be missed occasionally.
TRUE ___ or FALSE ___?

3. Consider the hardware-software codesign of a computer system containing an accelerator and a CPU that are connected by a shared bus. The system is to perform the following computation function on **pix**[N][M], an image array of size M **X** N. It places the results in another image array, **f**[N][M].

```
for (i = 0, i < M, i++)
  for (j = 0, j < N, j++)
    f[i][j] =  (pix[i-1][j-1] + pix[i-1][j] + pix[i-1][j+1] + pix[i][j-1] + pix[i][j+1] +
                pix[i][j] + pix[i+1][j-1] + pix[i+1][j] + pix[i+1][j+1])/9
```

The accelerator hardware has enough memory to store the **pix** and **f** image arrays during the above computation. Assume that **pix** array is loaded into the accelerator before the computation begins and **f** is written out at the end of total computation. Show a schedule for the CPU, accelerator and the shared bus assuming that the accelerator is inactive during the image data transfer. Assume that the image array transfer to or from accelerator takes the half of the above function computed by the accelerator hardware.

MARKS: 14

b) Fault-recovery is an important part of fault-tolerance and a number of schemes have been developed for fault recovery. Identify the scheme best suited to safety critical embedded systems. Justify your answer.

MARKS: 5

4. A variant of round robin scheduling is called selfish round robin scheduling. In selfish round robin, there is a maximum limit on the number of processes that can be placed in the round-robin queue (including the process being executed by the CPU). After that maximum is reached, newly entering processes are placed on a holding queue. Processes in the holding queue do not get any time slice of the CPU. When a process in the round-robin queue completes and leaves the system, the oldest process in the holding queue is allowed to enter the round-robin queue. Implement both the ordinary and selfish round-robin scheduling techniques for the following processes by showing the scheduling time lines for each process. Assume that a maximum of three processes can be placed in the round-robin queue at a time for selfish round robin and the time quantum q = 20.

MARKS: 20

Process #	Service Time	Arrival Time
0	80	0
1	40	15
2	60	20
3	30	80
4	40	95

5. **(a)** ARM Cortex M3 CPU has a much faster response time to multiple interrupts as compared to some other CPUs. Explain briefly how the faster response is achieved in Cortex M3 CPU?

MARKS: 5

(b) ARM CPUs (e.g. ARM7TDMI or Cortex M3) has been designed targeting handheld devices. Identify at least two specific features of ARM CPU programming/architecture that facilitate smaller size code? Justify your answer in detail.

MARKS: 5