MicroBlaze™ RISC 32-Bit Soft Processor

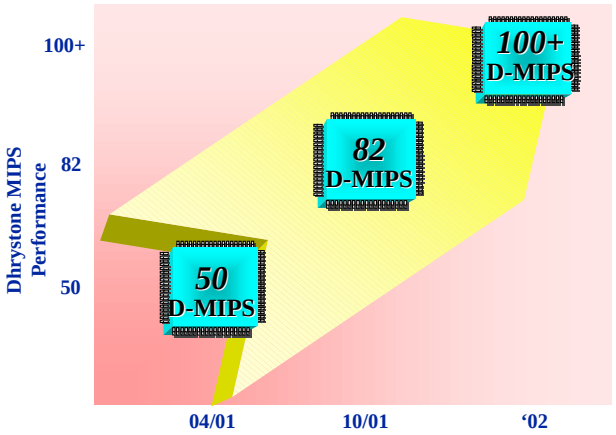
August 21, 2002 **Product Brief**

Features

- Supports Virtex, Virtex-E, Virtex-II Pro, Spartan-II, and Spartan-IIE devices
- Performance: 102 Dhrystone MIPS (D-MIPS) on Virtex-II Pro device at 150 MHz
- Minimum logic requirements: 900 logic cells
- 32-bit pipelined RISC architecture
- 32 x 32-bit general purpose registers
- Implementation in Virtex-II and later devices support hardware multiply
- Supports Local Memory Bus (LMB) for fast access of on-chip BRAMs
- Supports IBM CoreConnect On-chip Peripheral Bus (OPB) for accessing peripherals
- Processor peripherals compatible with PowerPC on Virtex-II Pro
- Complete hardware and software development tool and debug solution

Performance

The MicroBlaze processor is one part of an expanding array of processor functions that work together seamlessly to create the highest possible performance on a single FPGA. Beyond providing complete design solutions today, the MicroBlaze development platform will continue to support the designer in the future.



LogiCORE™ Facts	
Core Specifics	
Special Features	Up to102 D-MIPS at 150 MHz
Provided With Core	
Documentation	Embedded Software Tools Handbook and Embedded Processor IP Handbook
Design Files	Simulation Model Generator and Xilinx Generic Netlist Format (ngo netlist)
Design Tool Support	
Xilinx Implementation Tools	Xilinx ISE 5.1
Verification Tools	MicroBlaze GNU Debugger and Xilinx Microprocessor Debug (XMD) Tools
Support	
Please contact the Xilinx Hotline for technical support. Xilinx provides technical support for this LogiCORE Product when used as described in Product Documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices not listed above, or if customized beyond that allowed in the product documentation, or if any changes are made in sections of design marked as "DO NOT MODIFY".	

Table 1: MicroBlaze Speed, Performance, and Logic Cells in Xilinx Devices

Device Family	Speed	Performance	Logic Cells
Virtex-II Pro (-6)	150 MHz	102 D-MIPS	900
Virtex-II (-5)	125 MHz	82 D-MIPS	900
Virtex-E (-7)	75 MHz	49 D-MIPS	1050
Spartan-II (-6)	65 MHz	43 D-MIPS	1050
Spartan-IIE (-7)	75 MHz	49 D-MIPS	1050

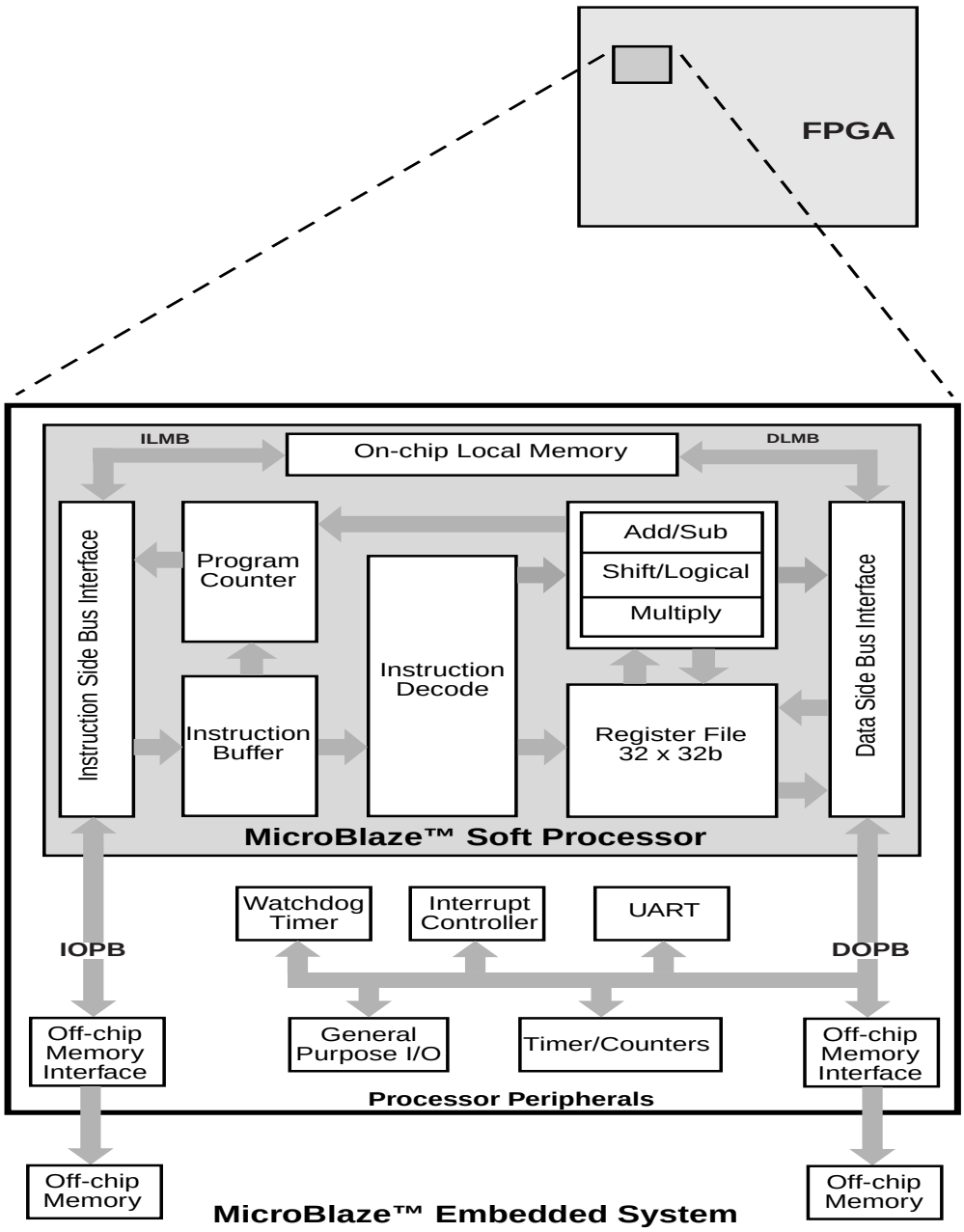


Figure 1: **MicroBlaze RISC 32-Bit Soft Processor System Interconnect Diagram**

General Description

An embedded system built around MicroBlaze is comprised of the following:

- MicroBlaze Soft Processor Core
- On-chip Local Memory
- Standard Bus Interconnects
- On-chip Peripheral Bus (OPB) Peripherals

A MicroBlaze system can range from a processor core with a minimum of local memory to a large system with many MicroBlaze processors, sizable external memory, and numerous OPB peripherals.

MicroBlaze applications can range from software-based simple state machines to complex controllers for Internet appliances or other embedded applications.

MicroBlaze Soft Processor Core

The MicroBlaze soft processor core is central to the MicroBlaze embedded system. This fast, efficient, 32-bit RISC processor includes the following features:

- Orthogonal instruction set
- Thirty-two 32-bit general purpose registers
- Separate instruction and data buses (Harvard architecture)
- Built-in interfaces to fast on-chip memory and to IBM's industry-standard On-chip Peripheral Bus (OPB)
- Implementations in Virtex-II and later devices support hardware multiply
- Optional full 32-bit barrel shifter

On-chip Local Memory

The Local Memory is a synchronous memory used primarily to access on-chip Block RAM.

Standard Bus Interconnects

The data side and instruction side bus interfaces each have an interface to local memory called the Local Memory Bus (LMB) and an interface to IBM's On-chip Peripheral Bus (OPB). You can build systems that strictly adhere to a Harvard architecture, or, to share resources, you can use a single OPB in conjunction with a bus arbiter (provided as a MicroBlaze peripheral).

The LMB bus provides guaranteed single-cycle access to on-chip block RAM. This simple, efficient, single-master bus protocol is ideal for interfacing to fast local memory. The OPB is a 32-bit wide multi-master bus that is ideal for connecting peripherals and external memory to the MicroBlaze processor core.

On-chip Peripheral Bus (OPB) Peripherals

OPB peripherals complete the MicroBlaze hardware system and provide functions such as the following:

- Watchdog Timer/Timebase
- General purpose Timer/Counters
- Interrupt Controller
- SRAM Controlller
- Flash Memory Controller
- ZBT Memory Controlller
- BRAM Controller
- DDR Controller
- SDRAM Controller
- UART Lite
- General purpose I/O
- SPI
- I2C (evaluation version)
- UART 16450/550 (evaluation version)
- Ethernet 10/100 MAC (evaluation version)

In addition, you can define and add peripherals for custom functions, or as an interface to a design residing in the FPGA.

Functional Description

The MicroBlaze 32-bit RISC soft processor is a true 32-bit processor supporting 32-bit bus widths. The core is a RISC-based engine with a 32-bit LUT RAM-based register file with separate instructions for data and memory access. The MicroBlaze processor supports both on-chip Block-RAM and/or external memory. All peripherals use the same CoreConnect OPB bus as the IBM PowerPC; therefore, the processor peripherals are compatible with PowerPC on Virtex-II Pro.

The MicroBlaze Embedded System, including the interconnected peripheral set, is shown in Figure 1.

Instruction Set Architecture

MicroBlaze uses two 32-bit instruction formats:

Type A is used for register-register instructions. It contains the opcode, one destination and two source registers.

Type B is used for register-immediate instructions. It contains the opcode, one dstination and one source registers, and a source 16-bit immediate value.

Registers

The MicroBlaze processor architecture is a fully orthogonal architecture. It has thirty-two 32-bit general purpose registers and two 32-bit special purpose registers (Program Counter and Machine Status Register).

Pipeline Architecture

MicroBlaze uses a three-stage pipeline architecture with fetch, decode, and execute stages.

Data forwarding, pipeline stall, and branches are resolved in the hardware automatically.

Load/Store Architecture

MicroBlaze can access memory in the following three data sizes: Byte (8 bits), Halfword (16 bits), and Word (32 bits). Memory accesses are always data-size aligned.

MicroBlaze is a Big-Endian processor and uses the Big-Endian address and labeling conventions when accessing memory.

Interrupts

When an interrupt occurs, the processor will stop the current execution to handle the interrupt request by branching to address of interrupt vector and store the address of the

instruction that was to be executed when the interrupt occurred. The MicroBlaze processor will also disable future interrupts by clearing the Interrupt Enable flag in the Machine Status Register.

Embedded Software Tools

Embedded system design consists of customization of the hardware and software component of the MicroBlaze processor.

The Embedded software tools (EST) consist of an integrated development environment called Xilinx Platform Studio (XPS). XPS includes the following:

- Hardware Tailoring Utilities: System Generator for Processors
- Software Tailoring Utilities: Library Generator and GNU Compiler Tools
- Simulation Tools
- Debug Tools

Xilinx Platform Studio

Xilinx Platform Studio (XPS) provides an integrated GUI for creating the software specification file for the Embedded Processor system. It also provides an editor and a project management interface to create and edit source code. It supports customization of SW libraries, drivers, interrupt handlers and compilation of user programs. XPS also supports customizing the hardware flow for the System Generator tool. It performs process management and dependency checking between the hardware and software flow by calling the tools in the correct order.

System Generator for Processors

Hardware generation is done with the Platform Generator for Processors (SGP) tool and the Microprocessor Hardware Specification (MHS) file. The user creates the MHS file to define the system architecture, the peripherals, and the embedded processors. The MHS file is given as an input to SGP to customize the hardware platform.

SGP generates the embedded processor system in the form of hardware netlists (HDL and EDIF files).

Library Generator

Software library generation is done with the Library Generator (LibGen) tool. For each MicroBlaze embedded processor instance, LibGen will configure the libraries and device drivers with the base addresses of the peripherals specified in the Microprocessor Software Specification (MSS) file. The user creates the MSS file to define the standard input/output devices, interrupt handler routines, and other related software features.

GNU Compiler Tools

The MicroBlaze tools include compiler, assembler and loader/linker. The MicroBlaze GNU compiler is an enhancement over the standard GNU tools and hence provides some additional options, which are specific to the MicroBlaze system.

Simulation Tools

The Simulation Model Generator (SimGen) tool generates and configures various simulation models for a specified hardware. It takes a Microprocessor Verification Specification (MVS) file as input. The MVS file has a reference to an MHS file that describes the hardware. The simulation tool to be used is also specified in the MVS file. The user can specify the HDL language in which the simulation models need to be generated. For each hardware instance, the user can also specify the simulation model to be used. SimGen produces a simulation model and a compilation script for vendor specific simulators.

Debug Tools

The debug tool chain for the MicroBlaze embedded system consists of the GNU Debugger (GDB) tool and the Xilinx Microprocessor Debug (XMD) Engine.

GDB is a powerful yet flexible tool which provides a unified interface for debugging/verifying MicroBlaze systems during various development phases.

The XMD Engine is a program that facilitates a unified GDB interface as well as a Tcl interface for debugging programs and verifying systems using the MicroBlaze processor. XMD offers users a choice of two execution targets: a hardware board or a cycle-accurate instruction set simulator.

System Requirements

- Xilinx ISE 5.1
- Windows 2000 or XP

Ordering Information

This Xilinx MicroBlaze RISC 32-bit Soft Processor kit is provided without a development board or with a Spartan-II, Spartan-IIE, Virtex-E, or Virtex-II development board. Please contact your local Xilinx sales representative for pricing and availability. Information on the sales office nearest you is available at http://www.xilinx.com/company/contact.htm.

Additional information on MicroBlaze is available on the Xilinx web site at http://www.xilinx.com/microblaze/.

To order Xilinx software or this product online, visit the Xilinx Silicon Xpresso Cafe at http://toolbox.xilinx.com/cgi-bin/xilinx.storefront/.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/21/02	1.0	Initial Xilinx release.