Problem-Set #3 – COE838

SoC Interconnections: Busses and NoC

Q-1. Suppose a processor has bus transactions that consist of cache line transfers. Assume that 80% of the transactions move a single line and occupy the bus for 20 cycles and 20% of the transactions move a double line (as in dirty line replacement), which takes 36 cycles. Assume that a cache miss (transaction) occurs after every 200 cycle.

i). Determine the mean bus transaction time.

Find the bus occupancy for in the case of a single processor system.

ii). Find the bus occupancy when there are four processors connected to the bus. What will be the contention time for in the case of a 4-processor System?

Q-2. Consider a split (address plus bidirectional data bus) bus is 32 + 64 bits wide. A typical bus transaction (read or write) uses a 32-bit memory address and 64-bit data transfer. The memory access time is 12 Cycles.

If four processors use the bus described above and ideally (without contention) each processor generates a transaction every 20 cycles.

i) What is the offered bus occupancy?

ii) Using the bus model without resubmissions, what is the achieved occupancy?

iii) Using the bus model with resubmissions, what is the achieved occupancy?

Q-3. Consider a wormhole routing based communication in a 2D 4×4 NoC. Determine the average number of clock cycles needed to transmit 256-bits of data where the width of NoC link is 16-wires, and the header size is of 64-bits.

Q-4. A static switching interconnect is implemented as a 4×4 torus (2-D) with wormhole routing. Each path is bidirectional with 32 wires; each wire can be clocked at 400 Mbps. For a message consisting of an 8-bit header and 128-bit "payload".

i) What is the expected latency (in cycles) for a message to transit from one node to an adjacent node?

ii) What is the average message latency (in cycles)?

iii) What is the total message transit time?

Q-5. Sketch the block diagram for a SoC with one processor, one SRAM, one ROM, one Counter/Timer block, A/D interface and one P-I/O section, all connected to a single bus without any bus bridges.

i). Is it appropriate for DMA to be supported or used in the above SoC?

ii). What modifications are needed if a 2nd processor core is to be added?

Is a second bus addition will be a good idea? Justify your answer.

Q-6. Consider a Network-On-Chip (NoC) based SoC interconnection.

i). What are the main differences between using multiple number of bus bridges and a network fabric?

ii). Describe a buffering technique for NoC links that might be used in an NoC?

iii). Consider various flow-control techniques for NoCs and Identify at least one of the flow control technique that can be preferably used in NoCs. List the main advantages of your selected flow control method.