COE838/EE8221: Systems-on-Chip Design
Course Management Summary (Winter 2025)

1. Introduction
This document provides a summary of the course outline while additional details will be made available at the SoC Design course webpage http://www.ecb.torontomu.ca/~courses/coe838/ and D2L. D2L will also be used for posting the labs and project submission as well as posting marks of labs, project, midterm, and final exam.

2. Course Objectives
This course will cover the basics of system-on-chip (SoC) design, hardware-software co-specification, co-synthesis, network-on-chip (NoC) systems and system-on-programmable-chip technologies. It provides the advanced knowledge required for system-on-chip design and development, multi-core architectures and embedded systems on a chip. Students will also be introduced to the main principles of embedded system-on-chip modeling and design using SystemC. Various SoC soft processor cores such as Nios-II, ARM Cortex-A9, and other CPU IPs will be explored. Various design tools including Altera Quartus II and other tools utilized in the labs and projects. Interconnection structures suitable for SoC design will be studied. On-chip buses (e.g., AMBA, Avalon, IBM Core-connect, etc.) and network-on-chip techniques will be discussed in detail. SystemC is also introduced for SoC modeling and analysis.

3. Textbooks and Other Teaching Material
1. M. Wolf, Computer as Components: Principles of Embedded Computing System Design, 3rd, or 4th edition Morgan Kaufmann-Elsevier Publishers 2012, 2016 ISBN 978-0-12-388436-7, ISBN 97801280538741.
2. Michael J. Flynn, Wayne Luk, Computer System Design: System on Chip, John Wiley, and Sons Inc. 2011, ISBN 978-0-470-64336-5
3. SystemC: From the Ground Up, 2nd Edition, D.C. Black, J Donovan, B. Bunton, A. Keist, Springer 2010, ISBN 978-0-387-69958-5.
4. On-Chip Communication Architectures, System on Chip Interconnect, S. Pascricha and N. Dutt, Morgan Kaufmann-Elsevier Publishers 2008, ISBN 978-0-12-373892-9.
5. Embedded Core Design with FPGAs, Z. Navabi, McGraw-Hill 2007, ISBN 978-0-07-147481-8 ISBN 0-07-147481-1.

Relevant review articles to be identified by the instructor and will be available on the course web or library.

4. Course Evaluation and Marking Scheme
- Labs/Project: **35%**
- Mid-Term Test: **25%** (Monday: February 10, 2025 --tentatively-- during lecture time slot)
- Final Exam: **40%**

5. Additional Information
i. Midterm Exams will also cover the corresponding labs to enforce individual lab attempts.
ii. Initial Labs will be mainly organized online/virtual on SoC modeling and design using SystemC and other tools.

6. Instructor
Dr. Gul N. Khan Professor - Computer Engineering
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Consultation Times: Monday 1:45PM to 3:0PM, or by Appointment
E-mail: gnkhan@torontomu.ca **Home Page:** https://www.ecb.torontomu.ca/~gnkhan/

Lab Instructors/Supervisors: Mr. Yoga Suhas Kuruba Manjunath, e-mail: yoga.kuruba@torontomu.ca

7. Course Outline and Schedule
- A tentative schedule of Lectures, Labs and project is provided. There may be some changes in the schedule.
- Amended schedule will be announced in the class and posted on D2L course website if required.
- For schedule updates, please check the announcement pages of the course website and D2L regularly.

Tentative Weekly Schedule

Weeks	Main Topics – Lectures:TRS1067	Labs/Project: ENG412
1	System on Chip (SoC) Introduction Introduction to SystemC	
2	Introduction to SystemC, Using SystemC for SoC Co-specification	**Lab1:** SystemC: Introduction and Tutorial
3	SystemC based SoC Modeling & Analysis Hardware-Software Co-synthesis	**Lab1:** Submission **Lab2a:** SoC Accelerator
4	Accelerators & Embedded System Design Basics of Chips and SoC ICs	**Lab2a:** Demo and Submission **Lab2b:** JPEG Encoder/Decoder SoC Design
5	Basics of Chips and SoC ICs IC Die Area & Cost, Area, and Power	**Lab2b:** Demo and Submission **Lab 3:** DE1-SoC Tutorial - Creating SoCs
6	***Mid-term Exam (Tentative February 10, 2025)***	*** Course Project Introduction**
Study Week Break	*** Start the Course Project ***	Study Week Break
7	NoC (Network-on-Chip) NoC based Interconnection	**Lab3:** Submission **Lab4:** Designing and Interfacing Custom IP
8	Regular and Application Specific NoC Topologies.	**Lab4:** Demo and Submission
9	System on Programmable Chips -- SoCs Introduction to HPS/FPGA Systems	**Lab4:** Demo and Submission
10	SoC Interconnection: On-Chip Busses: AMBA, IBM Core-connect, Avalon, etc.	**Demo of Project Progress**
11	Soft and other CPU Cores for SoC Multicore and MPSoC Architecture	**Project Interim Report**
12	SoC Verification - UVM (Universal Verification Methodology)	**Project Demo/Final Report**
13	SoC Application Case Studies. Catching up and Review	**Final Report**

Additional Points to be noted:

I. All the required course specific written reports including labs/assignments will be assessed not only on their technical/academic merit, but also on communication skills of the student as exhibited through these reports.
II. There will be a 5% penalty per day for late submission of labs or project.
III. The students must follow and adhere to all relevant university policies found in their online course shell in D2L and/or on the Senate website specifically Academic Integrity - Policy 60
IV. In the case of any virtual lecture/lab or project component, there may be some changes in the course contents and schedule.

Midterm exam is tentatively scheduled on Feb 10, 2025 during the lecture time slot.