Ryerson University
Department of Electrical and Computer Engineering
COE 608–Computer Organization and Architecture

Midterm Test **APRIL 27, 2016**

Name: _____ **Student Number:** _____ **Sec:**----------

Time limit: 2 hours 30 min Examiners: N. Mekhiel

Notes:
a) Closed book.
b) No calculators.
c) Answer all questions **in the space provided.**

Total Marks=80, each=20

Q1-1 Translate the following into C. Assume i is in register $s2, $s0 has base address of A[] array, $s1 has base address of B[] array and register $s9 has 1000.

```
        addi $s2, $0, $0
LOOP: sll $s3, $s2, 2
        add $s4, $s0, $s3
        add $s5, $s1, $s3
        lw $s6, 0($s4)
        lw $s7, 0(s5)
        add $s8, $s7, $s6
        sw  $s8, 0($s4)
        addi $s2, $s2, 1
        beq $s2, $s9, EXIT
        j  LOOP
EXIT:
```

4 i
& A[i]
& B[i]
A[i]
B[i]
A[i] → B[i].
A[i] = A[i] → B[i]
i + 1
if i == 1000

```
For (i=0; i <=1000; i++) {
    A[i] = A[i]+B[i];
}
```

Name:_____ Section:_____

Q1-2 Find the effective CPI for the above code if arithmetic and logic operations take 1 cycle, data transfer instructions take 3 cycles, and conditional branches take 2 cycles, unconditional branches takes 1 cycle.

$$CPI_{avg} = \frac{1\times 5 + 3\times 3 + 1\times 2 + 1\times 1}{10} = \frac{5+9+2+1}{10} = 1.7$$

(Arithm, Data)

Q1-3 Calculate the performance of the above code if the MIPS processor runs at 1 GHz

$$T = N \times CPI_{avg} * 1ns$$

$$= 1000 \times 1.7 \times 1\,ns \times 10 = 17000\,ns$$

$$= 17\,\mu s$$

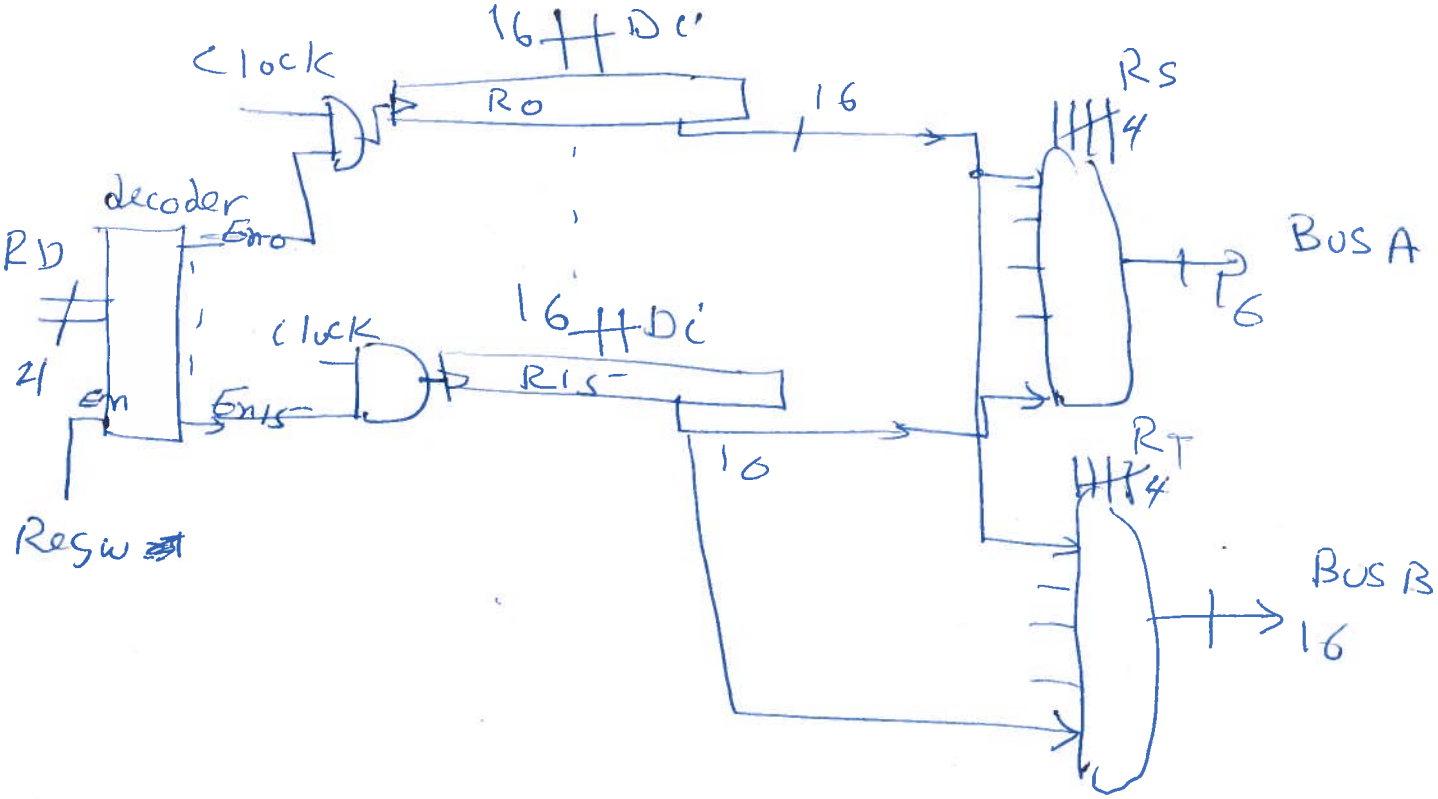
Q1-4 Find performance of above code if MIPS uses on chip cache for data transfers that improves it by 3 times but it slows down processor speed to 800 MHz.

$$T = 1000 \times (1\times 5 + 3\times 1 + 1\times 2 + 1\times 1) * 1.25\,ns$$

$$= 11 \times 1.25 \times 1000\,ns = 13.75\,\mu s$$

Name:_____ Section:_____

Q2-1 Design a Register File that consists of 16 Registers, each has 16 bits. Register File must have two READ ports, and one WRITE port. Draw a detailed schematic diagram.



Q2-2 Explain how a READ operations from Register 7, and Register 9 can be performed at the same time

Rs = 0111 , RT = 1001

Bus A = (R7)

Bus B = (R9)

Name:_____ Section:_____

Q2-3 Explain how a WRITE operation of 007E HEX to Register 2 is performed

0 0 7 E

DI = 0000 0000 0111 1110 , RD = 0010

RegW = 1

Q3-1 Convert the following decimal to IEEE754 FP format:

-.5625

S = 1 , 2^{-1} × .5625 = .1001

1	.1250
0	.2500
0	.5000
F	1.0

$= 1.001 \times 2^{-1}$

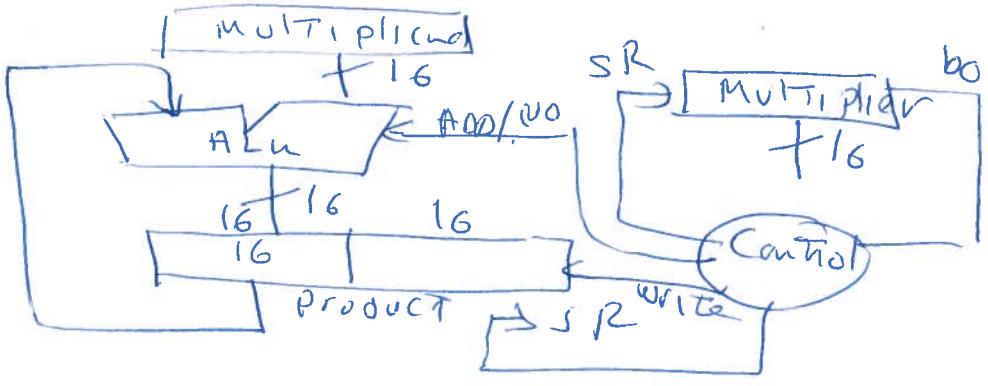
E = 126 − 127 64 32 16 8 4 2 1

E = 126 = 1 1 1 1 1 1 0

S E F

1 0 1 1 1 1 1 0 0 0 1 0 0 0 . . . 0

Q3-2 Draw a block diagram (hardware) to implement a multiplier system for 16 bits numbers



Name:_____ Section:_____

Q3-3 Calculate how long it takes for a single multiplication operation in the above syste assuming clock speed is = 1 GHz

16 operations, each consists of:
1- check LSb of Multiplier
2- ADD / no Add to Product
3- shift Right both product, Multiplieus
4- check if 16 operation done

= 64 cycles x 1 ns = 64 ns

Q4-1 For the Multicycle Data Path below, find the effective CPI running the code of Q1

Arithmetic takes 4 cycles F, D, ALu, write
lw Takes 5 cycles F, D, ALu, Mem, write
sw Takes 4 Cycles F, D, Alu, Mem
Cond branch Takes 3 cycles F, D, ALu
Uncond branch Takes F, D, Pcwrite 3 cycles

	Arithmetic	lw	sw	branch, j
	5	2	1	2
	4	5	4	3

$$CPI = \frac{5 \times 4 + 2 \times 5 + 1 \times 4 + 2 \times 3}{10} = 4 \text{ cycles}$$

Q4-2 Find the value of asserted control signals in each cycle when executing the following instruction:

sw $s8, 0($s4)

F: IoRD = 0, PcW = 1, MemR = 1, IRwrite = 1
ALuSrcA = 0 ALUSrc B = 1 ALu CnTL = ADD

D: Imm sign EXT

E: calculate Mem ADDRess ALuSrcA = 1, ALUSrc B = 2
ALu CnTL = ADD

Write: MemW = 1, IorD = 1

Name:_____ Section:_____

Q4-3 Identify all types of Hazards in the code of Q1 if it runs in a pipeline data path

1,2 RAW: sll, add in S3
1,3 " in S3
RAW 4,6 lw, add in S6
5,6 lw, add in S7
7,8 add, sw in S8
Control:- beq

Q4-4 If the pipeline uses forwarding, identify hazard stalls in Q1 that could not be eliminated by forwarding, then suggest a solution to get rid of stalls

lw S7, 0(S5)
add S8, S7, S6
1 cycle stall
schedule addi in between

lw S7, 0(S5)
addi $S2, $S2, 1
add S8, S7, S6

Name:_____ Section:_____