Ryerson University
Department of Electrical and Computer Engineering
COE 608–Computer Organization and Architecture

Final Exam **APRIL 23, 2018**

Name: _____ **Student Number:** _____ **Sec:**----------

Time limit: 2 hours 30 min

Examiners: N. Mekhiel

Notes:
a) Closed book.
b) No calculators
c) Answer all questions **in the space provided**.

Total Marks=80, each=20
(one bonus question)

Q1-1 Write MIPS Assembly for the following C code:-

```
For(i=0; i<1000 ; i++) {
 Y[i]  = A*X[i] + Y[i];
                    }
```

Assume that address of X[0] is at location 1000 and address of Y[0] is at location 10000, register $s0 is used for i and $s1 for A.

10

```
addi $s2, $0, 1000 ;   & X[0]
addi $s3, $0, 10000;   & Y[0]
addi $s0, $0, 0    ;   i = 0;
Loop: sll $s4, $s0, 2 ;   4i
add $s5, $s2, $s4;   & X[i]
add $s6, $s3, $s4;   & Y[i]
lw $t0, 0($s5);   X[i]
mult $t0, $t0, $s1;   A X[i]
lw $t1, 0($s6);   Y[i]
add $t1, $t0, $t1;   aX+Y
sw $t1, 0($s6);   Y[i]
addi $s1, $s1, 1 ;   i+1
slti $s7, $s1, 1000;   i<1000
bnz $s7, Loop
```

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Q1-2 Find the performance in time for the above code if each arithmetic and logic operations takes 1 cycle, data transfer instructions takes 4 cycles, and conditional branches takes 2 cycles, unconditional branches takes 1 cycle and processor runs at 2 GHz.

$T = 1000(7\times1 + 3\times4 + 1\times2) * .5 = 10.5\ \mu s$

3

Q1-3 Calculate the average CPI for the above code

$$CP = \frac{7\times1 + 3\times4 + 1*2}{11} = \frac{21}{11} \approx 2$$

2

Q1-4 Find performance gain of above code if MIPS uses 4 processors that could run 80% of the time in parallel.

$$T1 = \frac{.8\times10.5}{4} + .2\times10.5 = .4\times10.5 = 4.2\ \mu s$$

2

$$\text{Gain} = \frac{10.5}{10.5\times.4} = 2.5$$

2

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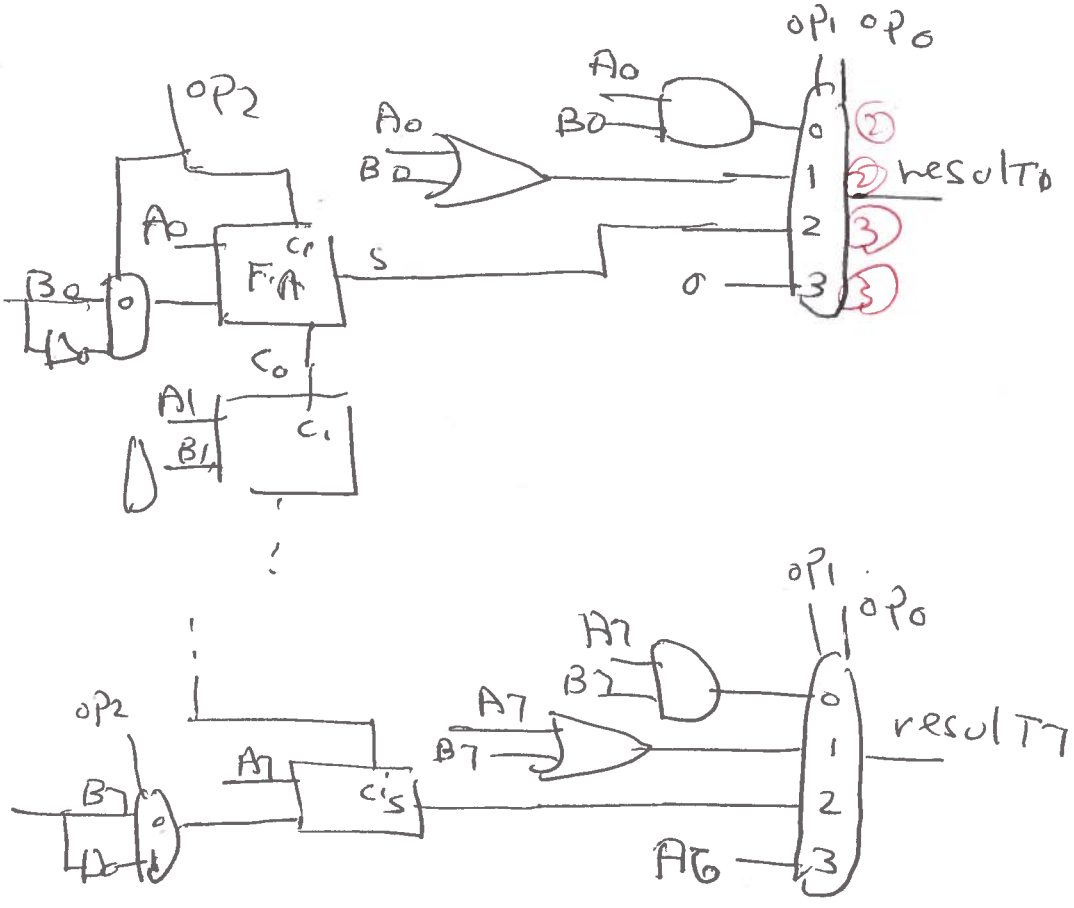
Q2-1 Design an ALU for 8 bit numbers A and B to performs operations based on the following op code:-

OP2	OP1	OP0	
0	0	0	AND
0	0	1	OR
0	1	0	ADD
1	1	0	SUB
1	1	1	SLL (shift logic left by 1 bit of A)

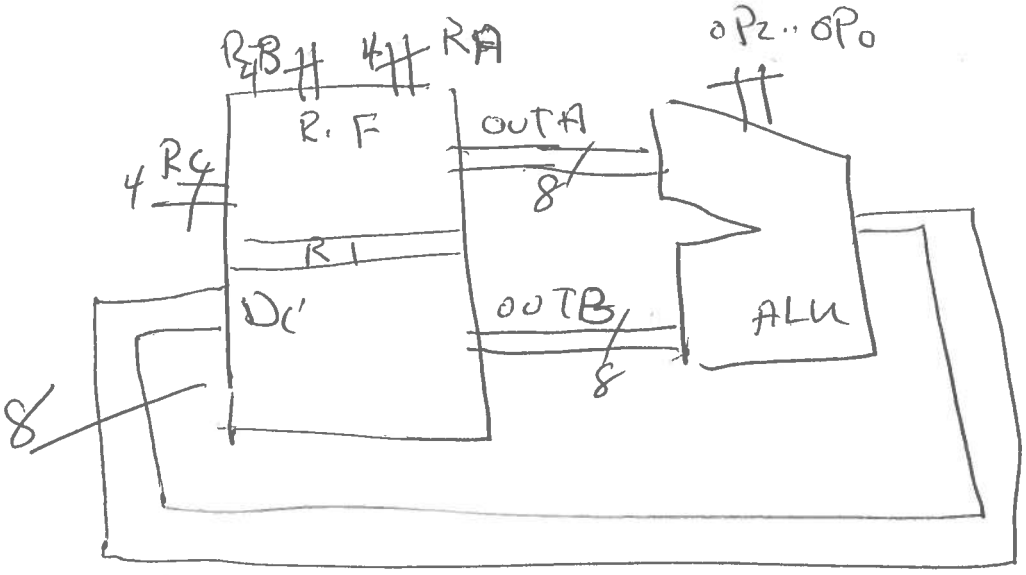
10



Name:_____ Section:_____

Q2-2 Assume using a register file of 16 registers each has 8 bits. It has two read ports labeld A, B and one write port labeled C. Draw a block diagram of a system that uses this register file and the above ALU to perform different operations on registers and the result is stored in one of registers (**no need to draw the logic gates inside ALU or RF**).

5



Name:_____ Section:_____

Q2-3 List the steps using op code above and register file operations as READ, WRITE and address of each register to produce 9*R1 and store the result in R7

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1- READ RA, RB RA = 0001

2- SHIFT A by 1 write to R2 = 2R1 RC = 0010
OP = 111

3- READ R2, R B RA = 0010

4- SHIFT A op = 111, write to R3 RC = 0011
R3 = 4R1

5- READ RA, RB RA = 0011

6- SHIFT A op = 111, write to R4 RC = 0100
R4 = 8R1

7- READ RA, RB = R1 0001, R4 = 0100

8- ADD opcode 010, write to R7 write to 0111
R7 = 9R1

Q3-1 Convert the following decimal to IEEE754 FP format:
-1.3125

8

S = 1

Fraction = .0101 $\times 2^0$

X 2	.3125
0	.625
1	.25
0	.5
1	0

number = 1.0101×2^0

E - 127 = 0 E = 127

1	01111111	01010 - - - 0
8	127	4

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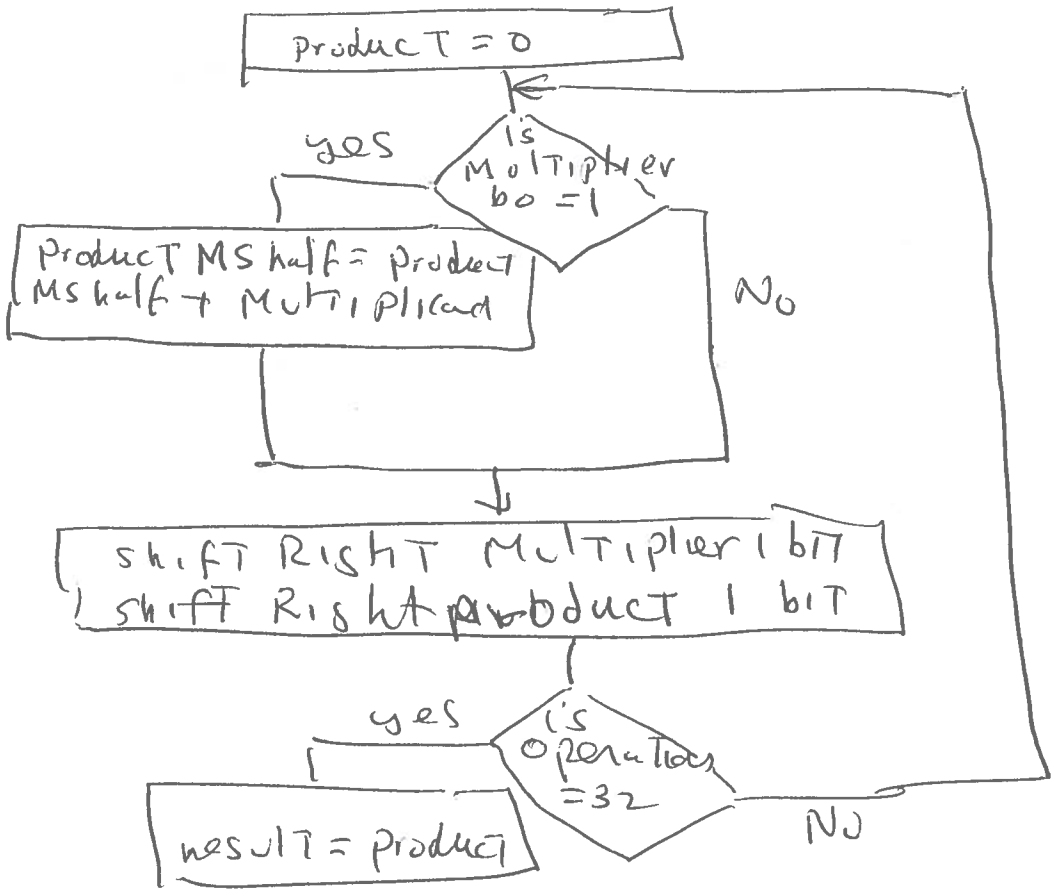
Q3-2 Draw a flow chart for algorithm to multiply two 32 bits numbers



8

Q3-3 Calculate how long it takes for a single multiplication operation in the above system assuming clock speed is = 2 GHz

$T = 4 \text{ steps} \times 32 = \frac{128}{2} = 64 \text{ ns}$

4

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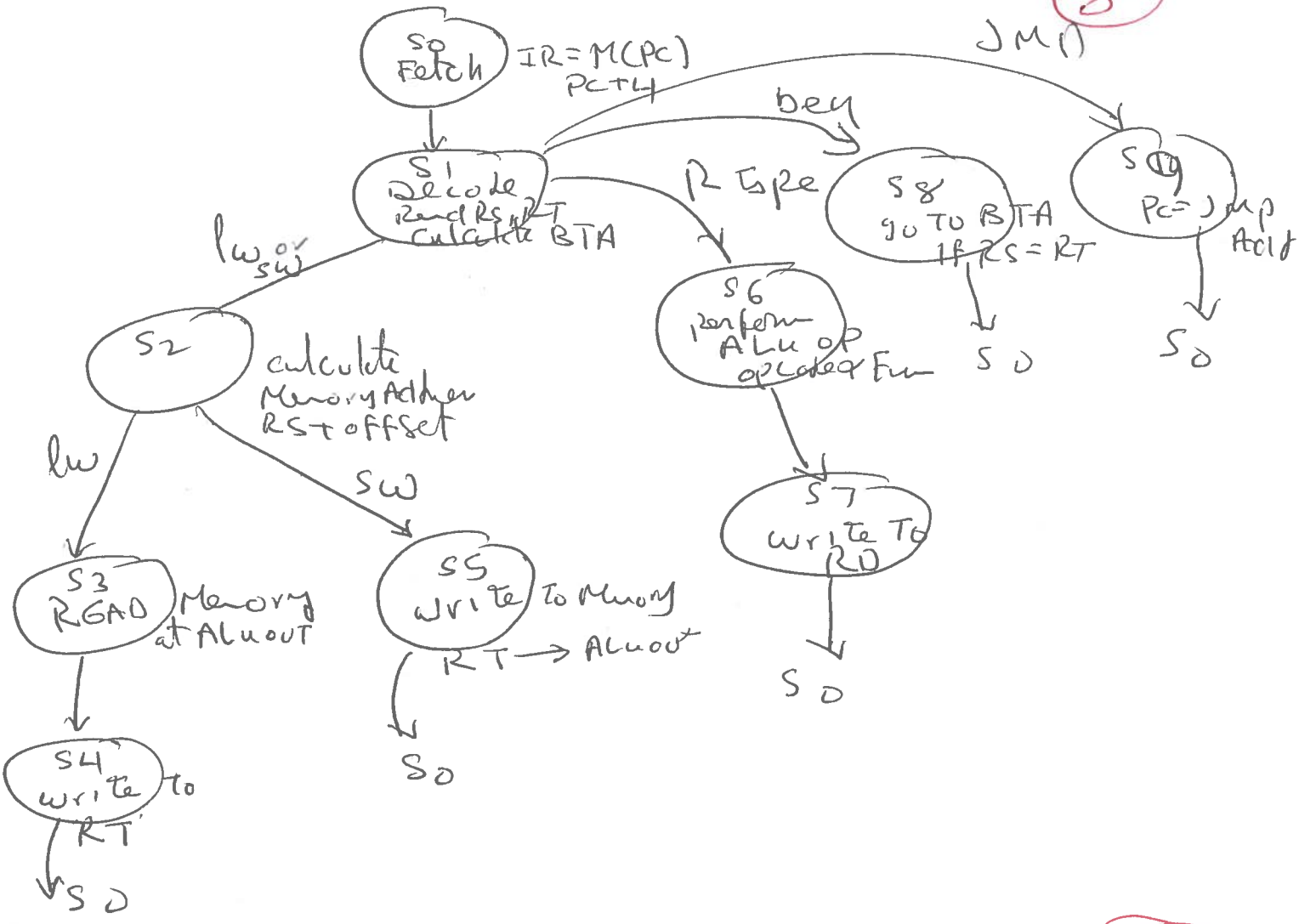
Q4-1 For the Multicycle Data Path below, draw the state diagram for the control unit

8



Q4-2 Find the value of asserted control signals in each cycle when executing the following instruction:

6

lw $s8, 0($s4)

S0: IorD=0, MemRead=1, IRW=1, ALUsrcA=0, ALUsrcB=1, ADD, PCW=1

S1: ALUsrcA=0, ALUsrcB=3, ALU ADD BTA

S2: ALUsrcA=1, ALUsrcB=2, ALU ADD RS+offset imm.

S3: MemRd=1 IorD=1

S4 = MemToReg=1, RegDst=0, RegW=1 write to RD

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Q4-3 Assume an application with the following frequency of use of instructions:-

lw 25%, sw 15%, arithmetic and logic 50%, conditional branch 10%

Find the performance improvement of using the multi cycle system compared to single cycle

single cycle takes 5 cycles

Multi cycle = .25 x 5 + .15 x 4 + .5 x 4 + .1 x 3

= 1.25 + .6 + 2 + .3 = 4.15 cycle

$\text{Gain} = \frac{5}{4.15} \approx 20\%$

6

Q5-Assume MIPS system uses pipelining with the following code:-

```
loop: lw  $t0, 0($s1)
      add $t1, $t0, $t2
      sw  $t1, 0($s1)
      addi $s1, $s1, 4
      bne  $s1, $s3, loop
```

Q5-1 Identify all the hazards in the above code

lw - add on t0 RAW

add — sw on t1 RAW

addi — bne on s1 RAW

bne Control

10

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Q5-2 Assume using forwarding and branch delay slot, reschedule the code to improve performance

```
Loop: lw  t0, 0(s1)
      addi s1, s1, 4
      add t1, t0, t2
      bne s1, s3, Loop
      sw  t1, -4(s1)
```

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